PAUL PELTZ JR

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AREAS OF INTEREST

My main focus is in new and emerging technologies and integrating them into production environments in order to increase operational efficiency. I enjoy working with new hardware architectures and the scaling challenges that are created by them. My passion is working in HPC as a systems engineer in order to provide a stable and highly optimized HPC platform for research scientists.

EXPERIENCE

Scalable Systems Engineer
April 2015 – Current

Los Alamos National Laboratory, HPC Design

Lead System Software Engineer on the ACES procurement of Trinity, which is a 110 cabinet Cray XC-40. Trinity consists of approximately 9500 Haswell, 9500 KNL nodes, DataWarp, and two 36PiB Sonexion filesystems. Since joining LANL my responsibilities include testing, integrating, and helping run acceptance on Trinity. Other responsibilities include providing Tier 3 support for the production team on multiple commodity clusters and Trinity, reviewing RFP and responses and then giving technical advisory on future HPC system procurements for LANL and other DOE laboratories, and collaborating with vendors on future hardware and software technologies. Currently leading a team to evaluate new system and configuration management software, cluster boot and provisioning, and DevOps/SRE tools to determine the best path forward in the HPC division.

HPC Systems Administrator
May 2013 – April 2015

National Institute for Computational Sciences, University of Tennessee, Knoxville

Lead Administrator for the Beacon system which is a 48 node Cray Cluster Solutions 300-AC cluster that utilizes four Intel Xeon Phi coprocessors per node. Responsible for the hardware, system software, and user support for Beacon. Also responsible for helping administer other NICS resources such as a Cray XT5 and Cray XC30. Lead Administrator on a small high throughput SeaMicro 15000 64 node cluster.

Member of the HPC Storage team that is responsible for maintaining the site wide 1.3 PB Lustre file system provided to all of the various NICS systems, the Sonexion direct attached storage appliance connected to the XC30, and other smaller storage appliances. Responsible for troubleshooting Lustre issues on the HPC resources. Developed and implemented a local 17TB SSD based Lustre on ZFS file system for Beacon.

Systems Administrator
May 1999 – May 2013

Innovative Computing Laboratory, University of Tennessee, Knoxville

Worked with researchers to understand new and pre-release hardware such as GPUs and Intel Xeon Phi coprocessors, and rapidly deployed new hardware to allow the researchers to begin exploring these new technologies. Responsible for a small 16 node cluster.

SKILLS AND PROFICIENCIES

Software
Ansible
CFEngine
CharlieCloud
Conman
Docker
Intel Compilers
Intel MPI
Ganglia
Gitlab/CI
Grafana
Kubernetes
Moab
Modules/Lmod
Nagios
nfsroot
OpenMPI
Powerman
Puppet
RT
Slurm
Subversion
SUSE OBS
TORQUE
Vagrant
VirtualBox
Warewulf

Hardware
ARM/Cavium
DDN
Cray X Series
Cray CCS 300
Intel Xeon Phi
InfiniBand
NetApp
NVIDIA GPUs
Omnipath
SeaMicro
Sonexion

Programming
Bash
Python
Go

Publications

Conference Publications:

How to Automate and not Manage under Rhine/Redwood May 2016
CUG '16, London, UK

Trinity: Architecture and Early Experience May 2016
CUG '16, London, UK

Invited Talks:

HPC Systems Acceptance: Controlled Chaos November 2016
SC'16, HPC Systems Professionals Workshop, Salt Lake City, UT

Original Publications in Peer-Reviewed Journals:

Benchmarking SSD-Based Lustre File System Configurations July 2014
XSEDE '14, Atlanta, Georgia

Rick Mohr and Paul Peltz, Jr.. 2014. Benchmarking SSD-Based Lustre File System Configurations. In *Proceedings of the 2014 Annual Conference on Extreme Science and Engineering Discovery Environment* (XSEDE '14). ACM, New York, NY, USA, Article 32, 2 pages. DOI=10.1145/2616498.2616544 http://doi.acm.org/10.1145/2616498.2616544

Best Practices for Administering a Medium Sized Cluster with Intel® Xeon Phi™ Coprocessors July 2014
XSEDE '14, Atlanta, Georgia

Paul Peltz, Jr. and Troy Baer. 2014. Best Practices for Administering a Medium Sized Cluster with Intel® Xeon Phi™ Coprocessors. In *Proceedings of the 2014 Annual Conference on Extreme Science and Engineering Discovery Environment* (XSEDE '14). ACM, New York, NY, USA, Article 34, 8 pages. DOI=10.1145/2616498.2616538 http://doi.acm.org/10.1145/2616498.2616538

Beacon: Deployment and Application of Intel Xeon Phi Coprocessors for Scientific Computing March/April 2015

Brook, R.G.; Heinecke, A.; Costa, A.B.; Peltz, P.; Betro, V.C.; Baer, T.; Bader, M.; Dubey, P., "Beacon: Exploring the Deployment and Application of Intel Xeon Phi Coprocessors for Scientific Computing," *Computing in Science & Engineering* , vol.17, no.2, pp.1,1, Mar.-Apr. 2015
DOI: 10.1109/MCSE.2014.113 http://dx.doi.org/10.1109/MCSE.2014.113

Integrating Apache Spark into PBS-Based HPC Environments July 2015
XSEDE '15, St. Louis, Missouri

Troy Baer, Paul Peltz, Jr.,Junqi Yin, Edmon Begoli. 2015. Integrating Apache Spark into PBS-Based HPC Environments. In *Proceedings of the 2015 XSEDE Conference: Scientific Advancements Enabled*

Operating Systems
Linux
OSX
Windows

Training/Certification
The Fundamentals of InfiniBand Fabrics from Mellanox

Active DOE Q Clearance

by Enhanced Cyberinfrastructure (XSEDE '15). ACM, New York, NY, USA, Article 34, 7 pages. DOI=10.1145/2792745.2792779 http://dx.doi.org/10.1145/2792745.2792779

Book Chapters

High Performance Parallelism Pearls

November 2014

Paul Peltz, Jr., Troy Baer, Vince Betro, Ryan Braby, Glenn Brook, and Karl Schulz. 2014. Integrating Intel Xeon Phi Coprocessors into a Cluster Environment. In *High Performance Parallelism Pearls*. Massachusetts: Elsevier, Book Chapter, 255-276. ISBN-13: 978-0128021187

EDUCATION

Political Science, Bachelor of Arts

2003

University of Tennessee, Knoxville

REFERENCES

Available Upon Request