How to Use SPEC Benchmarks for Decision Making

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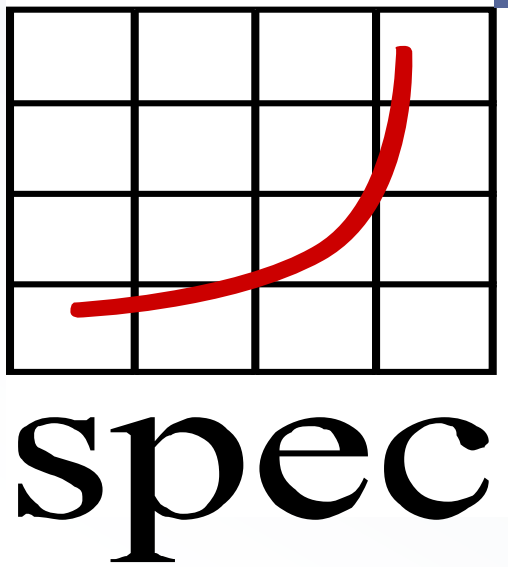


SPEC HPG:
https://www.spec.org/hpg
Tutorial Website:
https://www.olcf.ornl.gov/sc20-spec-hpg-tutorial

Contents

Contents

Benchmark components

SPEC benchmarks contain:

- benchmark codes
- benchmark workloads (input and output)
- SPEC tools
- run rule (every benchmark is different)

Benchmark components

SPEC Accel Benchmark Suites

benchmark

SPEC Accel suites:

- 34 benchmark codes in 3 suites

programming mode suites

OpenACC
15 codes

OpenMP target offload
same 15 codes with different directives

OpenCL
19 codes

results from different suites are not comparable

data set

test
(quickly test your binary)

train
(for feedback-directed optimization)

ref
(for production run and reporting)

```
Junjies-MBP16:ACCEL junjie$ ls
001.systest  114.mriq     122.cfd      128.heartwall  351.palm      357.csp       504.polbm      554.pcg       563.pswim
101.tpacf    116.histo    123.nw       140.bplustree  352.ep        359.miniGhost 514.pomriq     555.pseismic  570.pbt
103.stencil  117.bfs      124.hotspot  303.ostencil   353.clvrleaf  360.ilbdc     550.pmd        556.psp       ACCELacc.bset
104.lbm      118.cutcp    125.lud      304.olbm       354.cg        363.swim      551.ppalm      557.pcsp      ACCELocl.bset
110.fft      120.kmeans   126.ge       314.omriq      355.seismic   370.bt        552.pep        559.pmniGhost ACCELomp.bset
112.spmv     121.lavamd   127.srad     350.md         356.sp        503.postencil 553.pclvrleaf  560.pilbdc
Junjies-MBP16:ACCEL junjie$
```

Benchmark components

SPEC Accel Benchmark Suites

OpenACC/OpenMP4.5 Benchmarks	Language	Origin	Application Domain
ostencil	C	Parboil, University of Illinois	Thermodynamics
olbm	C	Parboil, University of Illinois, SPEC CPU2006	Computational Fluid Dynamics, Lattice Boltzmann
omriq	C	Rodinia, University of Virginia	Medicine
md	Fortran	Indiana University	Molecular Dynamics
palm	Fortran	Leibniz University of Hannover	Large-eddy simulation, atmospheric turbulence
ep	C	NAS Parallel Benchmarks	Embarrassingly Parallel
clvrleaf	C, Fortran	Atomic Weapons Establishment	Explicit Hydrodynamics
cg	C	NAS Parallel Benchmarks	Conjugate Gradient Solver
seismic	Fortran	GeoDynamics.org, University of Pau	Seismic Wave Modeling (PDE)
sp	Fortran	NAS Parallel Benchmarks	Scalar Penta-diagonal solver
csp	C	NAS Parallel Benchmarks	Scalar Penta-diagonal solver
miniGhost	C, Fortran	Sandia National Lab	Finite difference
ilbdc	Fortran	SPEC OMP2012	Fluid Mechanics
swim	Fortran	SPEC OMP2012	Weather
bt	C	NAS Parallel Benchmarks	Block Tridiagonal Solver for 3D PDE

SPEC Accel suites:

- the 15 codes in OpenACC suite
- real app or mini-app
- same codes later ported to OpenMP target offload suite
- coverages different scientific domains, different programming languages

Benchmark components

SPEChpc 2021 Benchmark Suites

benchmark

SPEChpc 2021 suites:

- 9~12 benchmark codes
- all codes support MPI, MPI+OpenMP, MPI+OpenACC, MPI+OpenMP target offload

workload

small
(scale up to 512 ranks)

medium
(scale up to ~8000 ranks)

large
(under development)

data set

test
(quickly test your binary)

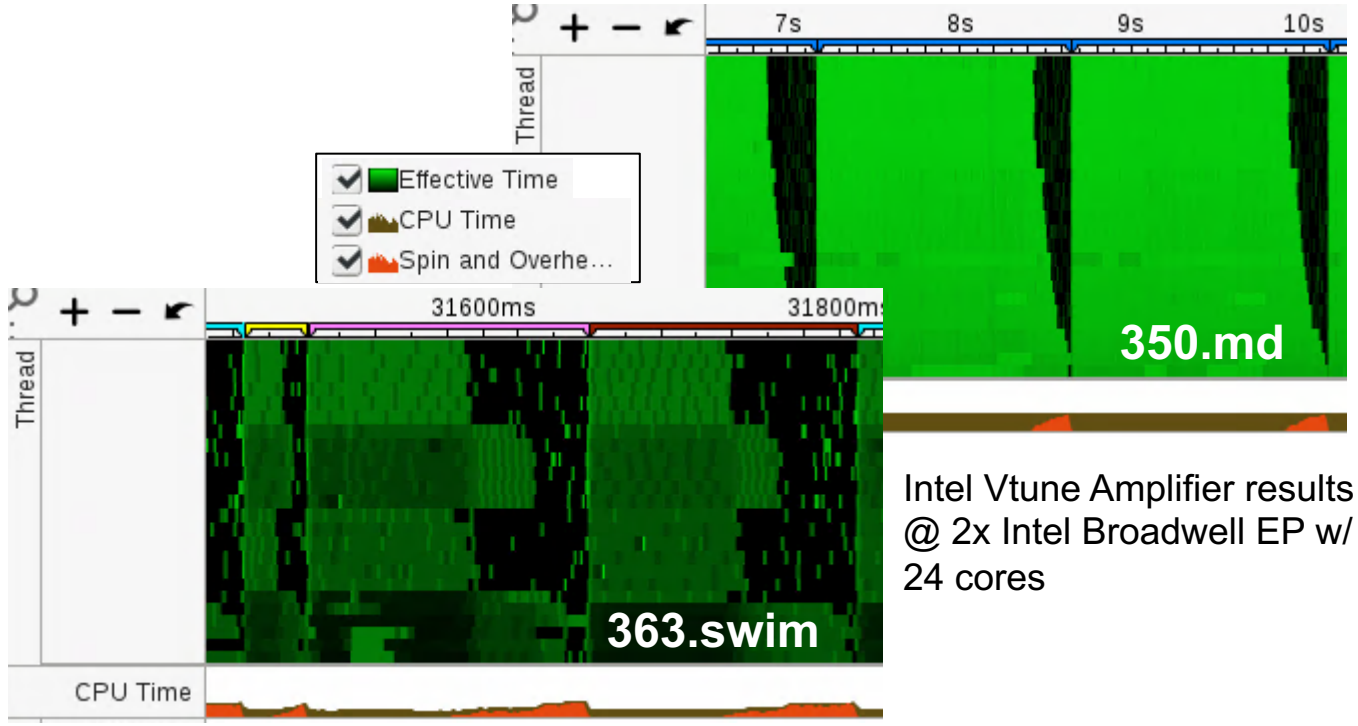
ref
(for production run)

For latest development of SPEChpc 2021
https://www.spec.org/hpc2021/

Benchmark components

- Codes are characterized during the selection process
- Coming from real-world applications
- May have completely different characteristics
- Identification: number and name
  - 350.md for example
- Documentation: website/ benchmark tree
  - Language, application domain,…

Intel Vtune Amp.	350.md	363.swim
CPI rate	0.698	1.634
CPU utilization	69 %	23.6 %
Memory bound	11.8 %	48.5 %
% of packed FP instr	9.7 %	100 %



Intel Vtune Amplifier results @ 2x Intel Broadwell EP w/ 24 cores

See SPEC HPG publication page for more performance studies:
https://www.spec.org/hpg/publications/

SPEC Tools

Tools provided to ensure consistent operation of benchmarks across variety of platforms

- **`runspec or runhpc`**
  - Primary tool in the suite
  - ***build, run, report all through this command*** (you don't manually run each code).
  - **Config file** needed for usage (with detailed instructions on building/running the benchmarks)
- **`rawformat`**
  - Results formatter needed for publishing SPEC results
- **`specmake, specperl, specsha512sum, specdiff, specpp`**, **`specrand`**, and many more
  - make, perl, sha512sum, etc.

Tool overview: http://spec.org/omp2012/Docs/tools-build.html

links

Config Files

- Contain instructions
  - Building benchmarks
  - Running them
  - Description of system under test

Key for reproducibility!

- How to write a config file?
  - Often start off using a config file that someone else has previously written[1]
    - example config in `$SPEC/config/`
    - from SPEC result submissions similar to your system[2]
  - Write your own[3]

Source: as of May 2018[2]

Test Sponsor	System Name	Base Threads	Processor				Results	
			Enabled Cores	Enabled Chips	Cores/ Chip	Threads/ Core	Base	Peak
Intel	Intel Server System R2208WFTZS (2 x Intel Xeon Platinum 8180, DDR4-2666, SMT ON Turbo ON) HTML | CSV | Text | PDF | PS | Config	112	56	2	28	2	21.1	25.5
Lenovo Global Technology	ThinkSystem SR950 HTML | CSV | Text | PDF | PS | Config	224	112	4	28	2	40.2	Not Run
Oracle Corporation	SPARC T7-4 HTML | CSV | Text | PDF | PS | Config	256	128	4	32	8	26.4	27.9
RWTH University Aachen	NEC HPC 1812Rg HTML | CSV | Text | PDF | PS | Config	24	24	2	12	2	7.22	Not Run
RWTH University Aachen	NEC HPC 1812Rg HTML | CSV | Text | PDF | PS | Config	48	24	2	12	2	7.65	Not Run
RWTH University Aachen	NEC HPC 1812Rg HTML | CSV | Text | PDF | PS | Config	144	144	8	18	2	33.6	Not Run
RWTH University Aachen	NEC HPC 1812Rg HTML | CSV | Text | PDF | PS | Config	72	144	8	18	2	19.5	Not Run
RWTH University Aachen	NEC HPC 1812Rg HTML | CSV | Text | PDF | PS | Config	36	144	8	18	2	9.97	Not Run
RWTH University Aachen	NEC HPC 1812Rg HTML | CSV | Text | PDF | PS | Config	18	144	8	18	2	5.23	Not Run

[1] https://www.spec.org/accel/docs/runspec.html#about_config
[2] https://www.spec.org/omp2012/results/omp2012.html
[3] https://www.spec.org/accel/docs/config.html

links

Config Files

Header section
- Usually runspec flags

```
# Before any instances of "default"
####################################################
# what to do: build, validate = build+ run+ check+ report
action        =  validate
# Number of iterations of a test
iterations    =  1
# Tuning levels: base, peak
tune          =  base
# Dataset size: test, train, ref
size          =  test
# Environment variable will be set using "ENV_*"
env_vars      =  1
# Output format: all, pdf, text, html and so on
output_format =  text
flagsurl      =  $[top]/../flagsfile/Intel.xml
teeout        =  yes

# Run benchmarks according to your specific system config
# The variable "command" is the command used by spec
# submit = <system command> $command

#submit = numactl -p 1 $command
#submit = aprun -n 1 $command
```

Compiler Specification

```
####################################################
# Software information
####################################################
# Compilers. Using PGI compiler for example
default=default=default=default:
CC                = pgcc
CXX               = pgc++
FC                = pgfortran

# Environment variables at runtime
ENV_PGI_ACC_BUFFERSIZE = 8M
```

Compiler Flags
- Base & Peak (optional)
- Portability

```
####################################################
# Base
####################################################

openacc=base=default=default:
OPTIMIZE      = -fast -Mfprelaxed
FOPTIMIZE     = -acc -ta=tesla:cc35,cuda5.5
COPTIMIZE     = -acc -ta=tesla:cc35,cuda5.5

####################################################################
# Portability flags for each benchmark
# Following flag should not have any impact on performance.
####################################################################

359.miniGhost=default=default=default:
EXTRA_LDFLAGS += -Mnomain

####################################################################
# Peak
####################################################################
350.md=peak=default=default:
FOPTIMIZE = -acc -ta=tesla:cc35,cuda5.5,maxregcount:48

352.ep=peak=default=default:
FOPTIMIZE = -acc -ta=tesla:cc35,llvm

359.miniGhost=peak=default=default:
FOPTIMIZE = -acc -ta=tesla:cc35,cuda5.5,maxregcount:32
COPTIMIZE = -acc -ta=tesla:cc35,cuda5.5,maxregcount:32

####################################################################
# Hardware and software information for the machine under test.
# This information will  be extracted for a reportable run.
# An example configuration can be copied from the website
# https://www.spec.org/accel/results/accel_acc.html
####################################################################
company_name     = SPEC Tutorial Company
test_sponsor     = SPEC Tutorial Sponsor
tester           = SPEC Tutorial Tester
license_num      = SPEC Tutorial License
machine_name     = SPEC Tutorial Machine
```

Host Information

```
####################################################################
# # HOST Hardware information
####################################################################
# default=default=default=default:
hw_avail = Nov-2013
hw_cpu_name = Intel Core i7-3930K
hw_cpu_mhz = 3200
hw_cpu_max_mhz = 3800
hw_fpu = Integrated
hw_nchips = 1
hw_ncores = 6
hw_ncoresperchip = 6
hw_nthreadspercore = 2
hw_ncpuorder = 1 chip
hw_pcache = 32 KB I + 32 KB D on chip per core
hw_scache = 256 KB I+D on chip per core
```

Accelerator Information

```
####################################################################
# # Accelerator Hardware information
####################################################################

hw_accel_model = Tesla K40c
hw_accel_vendor = NVIDIA
hw_accel_name = NVIDIA Tesla K40c
hw_accel_type = GPU
hw_accel_connect = PCIe 3.0 16x
hw_accel_ecc = Yes
hw_accel_desc000 = GPU Boost set to use a graphic clock frequency
hw_accel_desc001 = of 810 MHz. See notes below.
```

MD5 section
- Automatically-generated

```
####################################################
# MD5 section. It will be created by SPEC automatically.
# It is used by SPEC to check whether an executable if
# available is created using the current compiler and flags
# settings.
####################################################
```

Config Files

```
############################################################
# Software information
############################################################

# Compilers.
default=default=default=default:
CC             =  mpicc
CXX            =  mpic++
FC             =  mpifortran

############################################################
# Base
############################################################

openacc=base=default=default:
OPTIMIZE     = -fast -Mfprelaxed
FOPTIMIZE    = -acc -ta=tesla:cc70,cuda10.1
COPTIMIZE    = -acc -ta=tesla:cc70,cuda10.1
```

Named section

```
benchmark[,…]=tuning[,…]
=extension[,…]=machine[,…]:
```

- **Settings for base runs**
- **same flag for all**
- Compiler flags or environment variables

Config Files

```
# Environment variables at runtime
ENV_PGI_ACC_BUFFERSIZE = 8M


##############################################################
# Portability flags for each benchmark
# Following flag should not have any impact on performance.
##############################################################
```

Environment variables
- Active if `env_vars` is set to `1` (see prior slides)
- Need to start with `ENV_`

Set portability flags if benchmark cannot be built/ execute correctly w/o these flags.

Other typical portability flags: language standards (-std=c99), Fortarn format (-free), memory models (-mcmodel=medium)

SPEC Accel OpenACC current doesn't need portability flag with PGI.

Config Files

```
############################################################################
# Hardware and software information for the machine under test.
# This information will  be extracted for a reportable run.
# An example configuration can be copied from the website
# https://www.spec.org/accel/results/accel_acc.html
############################################################################

company_name     = SPEC Tutorial Company
test_sponsor     = SPEC Tutorial Sponsor
tester           = SPEC Tutorial Tester
license_num      = SPEC Tutorial License
machine_name     = SPEC Tutorial Machine

hw_vendor        = NEC
hw_avail         = NOV-2016
hw_cpu           = Intel Xeon E5-2650 v4
hw_cpu_mhz       = 2200
hw_cpu_max_mhz   = 2900
```

HW & SW description

- Needed only for reportable runs
- `runspec` tools captures information in submission file
- Very detailed information

Information on host configuration, e.g. CPU

Config Files

```
############################################################################
# HOST Hardware information
############################################################################ default=default=default=default:
hw_avail = Nov-2013
hw_cpu_name = Intel Core i7-3930K
hw_cpu_mhz = 3200
hw_cpu_max_mhz = 3800
hw_fpu = Integrated
hw_nchips = 1
hw_ncores = 6
hw_ncoresperchip = 6
hw_nthreadspercore = 2
hw_ncpuorder = 1 chip
hw_pcache = 32 KB I + 32 KB D on chip per core
hw_scache = 256 KB I+D on chip per core
hw_tcache = 12 MB I+D on chip per chip


############################################################################
# Accelerator Hardware information
############################################################################

hw_accel_model = Tesla K40c
hw_accel_vendor = NVIDIA
hw_accel_name = NVIDIA Tesla K40c
hw_accel_type = GPU
hw_accel_connect = PCIe 3.0 16x
hw_accel_ecc = Yes
```

Performance critical aspects of Host and Accelerator are documented

Config Files

```
############################################################
# Software information
############################################################
default=default=default=default:
sw_avail = Feb-2014
sw_compiler = PGI Accelerator Server Complete, Release 14.2
sw_accel_driver = NVIDIA UNIX x86_64 Kernel Module 319.60
```

Information on software configuration, e.g. compilers

```
############################################################
# MD5 section. It will be created by SPEC automatically.
# It is used by SPEC to check whether an ex
# the current compiler and flags settings.
############################################
```

MD5 section

- Automatically generated by SPEC tools
- Used to check whether an executable is created using the current settings

SPEC Score

- Each benchmark component will have a performance “ratio”.
- “ratio”=speed up comparing to a reference machine (ratio of runtime)
- SPEC Score = geometric mean of “ratio” from all benchmark components
- SPEC Score of reference machine is “1”
- Higher is better, easy to understand

- Reference machines
  - For SPEC OMP2012
    - Sun Fire X4140, 2xAMD Opteron 2384, 8 cores, 2 chips, 4 cores/chip, 2.7 GHz
  - For SPEC Accel
    - SGI C3108-TY11, NVIDIA Tesla C2070, Intel Xeon E5620 2.4GHz

Run rules

fair, objective benchmarking and full reproducibility.

(full run rule is 20 page doc, only key points here)

- Most benchmarks forbids source code changes
  - rely on compiler and runtime for performance optimization
  - instead of testing programmer's optimization skill, SPEC gauges what the software stack can do
  - SPEC Accel allows changes in directives for peak runs

OpenMP: https://www.spec.org/omp2012/docs/runrules.html
MPI: https://www.spec.org/mpi/docs/runrules.html
ACCEL: https://www.spec.org/accel/docs/runrules.html

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  - SPEC Accel allows changes in directives for peak runs
- Base vs Peak:
  - Base run: must have the same compiler flags for all benchmark components
  - Peak run: compiler flags can be tuned for reach individual benchmark

OpenMP: https://www.spec.org/omp2012/docs/runrules.html
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  - instead of benchmarking programmer's optimization skill, SPEC gauges what the software stack can do for regular users
  - SPEC Accel allows changes in directives for peak runs
- Base vs Peak:
  - Base run: must have the same compiler flags for all benchmark components
  - Peak run: compiler flags can be tuned for reach individual benchmark
- System under test needs to be fully documented for reproducibility
- Benchmark results are submitted to SPEC for peer review before going public (a two-week review period)
- All official SPEC results are published on SPEC website

OpenMP: https://www.spec.org/omp2012/docs/runrules.html
MPI: https://www.spec.org/mpi/docs/runrules.html
ACCEL: https://www.spec.org/accel/docs/runrules.html

Flags - From base to peak runs

- Modifying the config file
  - Once you have a config file that runs on your system, it is easy to modify it
  - E.g. `peak` optimizations for better performance

- Example:

SPEC® OMPG2012 Result

Copyright 2012-2016 Standard Performance Evaluation Corporation

Hewlett Packard Enterprise (Test Sponsor: HPE)	SPECompG_base2012 = 47.7
Integrity Superdome X (288 core, 2.50 GHz, Intel Xeon E7-8890 v3)	SPECompG_peak2012 = 55.3

OMP2012 license:	1	**Test date:**	Apr-2016
Test sponsor:	HPE	**Hardware Availability:**	Oct-2015
Tested by:	HPE	**Software Availability:**	Feb-2016

350.md: -O3 -openmp -ipo -xCORE-AVX2 -fno-alias -opt-malloc-options=1 -fp-model fast=2 -no-prec-div -no-prec-sqrt -align array64byte

351.bwaves: -O3 -openmp -ipo -xCORE-AVX2 -fno-alias -fp-model fast=2 -no-prec-div -no-prec-sqrt -align array64byte

357.bt331: Same as 351.bwaves

360.ilbdc: basepeak = yes

362.fma3d: -O3 -openmp -ipo -xCORE-AVX2 -fno-alias -align array64byte

363.swim: -O3 -openmp -ipo -xCORE-AVX2 -fno-alias -opt-streaming-stores always -opt-malloc-options=3 -align array64byte

370.mgrid331: -O3 -openmp -ipo -xCORE-AVX2 -fno-alias -opt-malloc-options=3 -fp-model strict

SPEC Peak run example: OMP Config File

Just show you how a peak run will look like:

```
##########################################################
# Peak
##########################################################
default=peak=default=default:
OPTIMIZE    = -O3 -qopenmp -ipo -xCORE-AVX2 -no-prec-div
COPTIMIZE   = -ansi-alias
CXXOPTIMIZE = -ansi-alias
FOPTIMIZE   = -align

# [..] Environment variables

350.md=peak=default=default:
OPTIMIZE=-O3 -qopenmp -ipo -xCORE-AVX2 -ansi-alias -qopt-malloc-options=1
FOPTIMIZE=-fp-model fast=2 -no-prec-div -no-prec-sqrt -align array64byte

363.swim=peak=default=default:
OPTIMIZE=-O3 -qopenmp -ipo -xCORE-AVX2 -ansi-alias -qopt-streaming-stores always
         -qopt-malloc-options=4
threads=24
```

FP optimizations

memory optimizations

- `-qopt-malloc-options`: alternate algorithm for malloc
- `-fp-model fast=2`: aggressive optimization on FP computations
- `-no-prec-sqrt`: less precise square root computations/ more performance
- `-align array64byte`: align arrays to 64 Byte
- `-qopt-streaming-stores always`: use non-temporal stores (write through)

Flags - From base to peak runs

Peak optimization rules: https://www.spec.org/omp2012/Docs/runrules.html#section2.4
Published results OMP2012: https://www.spec.org/omp2012/results/omp2012.html

Peak runs

- Set of optimizations individually selected for each benchmark
  - e.g. different compilers, flags
- Called “aggressive compilation”
- Most published results do not contain peak, too much work
- lots of room to explore
- peak results are typically from vendors (e.g. showcase higher performance during RFP competition)

Practice

You will be able to play with the benchmarks in the hands-on section coming next.

Contents

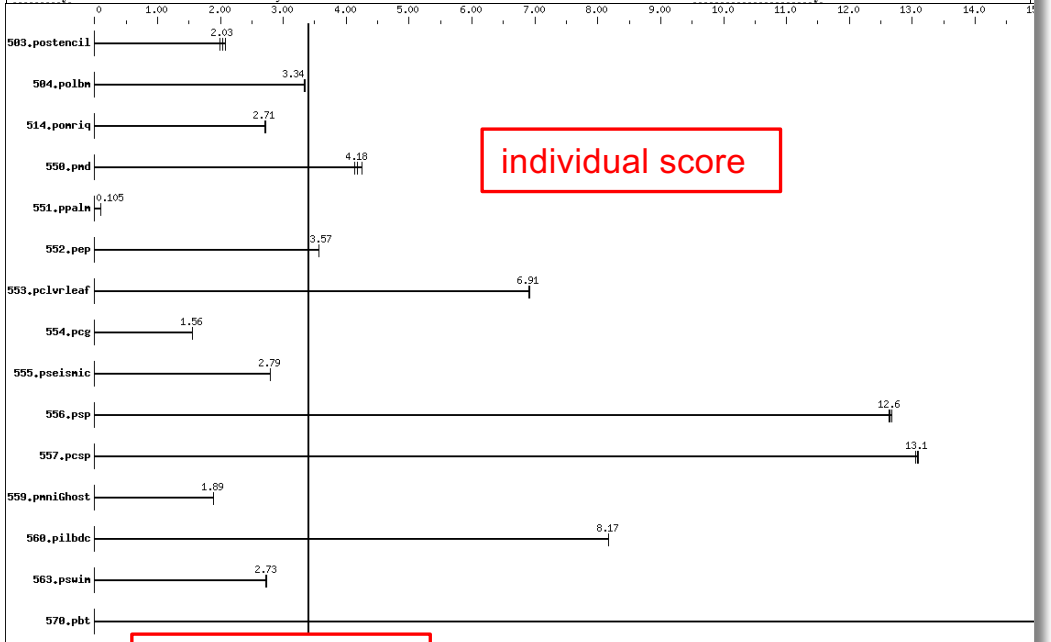
SPEC® ACCEL™ OMP Result

total score

Colfax International (Test Sponsor: Indiana University)
Xeon Phi 7210
Ninja Developer Platform Pedestal: Liquid Cooled

SPECaccel_omp_base =	3.40
SPECaccel_omp_energy_base =	4.54
SPECaccel_omp_peak =	Not Run
SPECaccel_omp_energy_peak =	--

ACCEL license:	3440A	**Test date:**	May-2017
Test sponsor:	Indiana University	**Hardware Availability:**	Aug-2016
Tested by:	Indiana University	**Software Availability:**	Jan-2017



individual score

hardware

Hardware

CPU Name:	Intel Xeon Phi 7210
CPU Characteristics:	Simultaneous multithreading (SMT) on, Turbo off.
CPU MHz:	1300
CPU MHz Maximum:	1300
FPU:	Integrated
CPU(s) enabled:	64 cores, 1 chip, 64 cores/chip, 4 threads/core
CPU(s) orderable:	1 to 1 chip
Primary Cache:	32 KB I + 32 KB D on chip per core
Secondary Cache:	1 MB I+D on chip per tile (2 cores)
L3 Cache:	None
Other Cache:	None
Memory:	96 GB (6 x 16 GB 2Rx8 PC4-2400T-REB-11, ECC) + 16 GB MCDRAM
Disk Subsystem:	Intel S3510 SSD 800GB, SATA3
Other Hardware:	None

Accelerator

Accel Model Name:	Xeon Phi 7210
Accel Vendor:	Intel
Accel Name:	Xeon Phi 7210
Type of Accel:	CPU
Accel Connection:	N/A
Does Accel Use ECC:	Yes
Accel Description:	Second generation Xeon Phi self-bootable CPU, SMT on, Turbo off, flat DDR4+MCDRAM
Accel Driver:	N/A

Software

Operating System:	CentOS Linux release 7.2.1511 (Core) 3.10.0-327.13.1.el7.xppsl_1.3.3.151.x86_64
Compiler:	Intel Parallel Studio XE 2017 Update 1 for Linux, Version 17.0.1.132 Build 20161005
File System:	ext4
System State:	Run level 3 (multi-user with networking)
Other Software:	None

Power

Power Supply:	750W

software

Power Supply Details:	Seasonic SSR-750RM Active PFC F3
Max. Power (W):	
Idle Power (W):	
Min. Temperature (C):	

power measurement device

Power Analyzer

Power Analyzer:	156.56.179.146:8888
Hardware Vendor:	ZES Zimmer
Model:	ZES LMG450:4-Channel
Serial Number:	01001849
Input Connection:	RS232 USB adapter
Metrology Institute:	NIST (National Institute of Standards and Technology)
Calibration By:	ZES Zimmer
Calibration Label:	3783190001e
Calibration Date:	02.20.2017
PTDaemon Version:	1.8.1 (a497ea15; 2016-12-20)
Setup Description:	connected to the single power supply that powers the system
Current Ranges Used:	0.0A
Voltage Range Used:	130V

Temperature Meter:	
Hardware Vendor:	
Model:	
Serial Number:	
Input Connection:	
PTDaemon Version:	
Setup Description:	

raw data

Results Table

Benchmark	Seconds	Ratio	Energy (kJ)	Maximum Power	Average Power	Energy Ratio	Seconds	Ratio	Energy (kJ)	Maximum Power	Aver Pow
503.postencil	52.4	2.08	12.9	254	245	2.77	54.5	2.00	13.3	252	2
504.polbm	36.4	3.35	9.79	272	269	4.01	36.6	3.33	9.80	272	2
514.pomriq	229	2.71	59.8	267	261	3.09	228	2.72	59.3	267	2
550.pmd	56.6	4.26	15.2	270	268	4.86	**57.6**	**4.18**	**15.4**	**271**	2
551.ppalm	**5182**	**0.105**	**690**	**157**	**133**	**0.226**	5183	0.105	690	157	1
552.pep	64.7	3.57	15.0	234	233	4.87	64.8	3.57	15.2	236	2
553.pclvrleaf	166	6.92	40.9	250	247	8.46	166	6.90	40.9	250	2
554.pcg	213	1.56	36.8	221	173	2.55	214	1.56	36.7	220	1
555.pseismic	**101**	**2.79**	**21.2**	**275**	**210**	**4.33**	101	2.79	21.2	275	2
556.psp	**64.7**	**12.6**	**14.7**	**236**	**227**	**15.5**	64.5	12.7	14.7	235	2
557.pcsp	**65.6**	**13.1**	**16.3**	**261**	**249**	**14.7**	65.8	13.1	16.3	259	2
559.pmniGhost	210	1.89	41.3	259	197	2.77	**210**	**1.89**	**41.1**	**260**	1
560.pilbdc	**80.0**	**8.17**	**22.1**	**285**	**276**	**8.87**	80.0	8.17	22.3	286	2
563.pswim	**58.1**	**2.73**	**13.1**	**228**	**225**	**3.98**	58.4	2.72	13.2	228	2
570.pbt	51.6	15.1	10.5	207	204	19.8	**51.4**	**15.2**	**10.6**	**208**	2

Results appear in the order in which they were run. Bold underlined text ind

Submit Notes

```
The config file option 'submit' was used.
submit = numactl -p 1 $command
```

Platform Notes

```
Sysinfo program /home/lijunj/spec/accel-test/75/Docs/sysinfo
$Rev: 6965 $ $Date:: 2015-04-21 #$ c05a7f14b1b1765e3feldf68447e8a35
running on knl1.uits.indiana.edu Tue May  2 11:07:12 2017

This section contai
some common utiliti
  http://www.spec.o

From /proc/cpuinfo
   model name : Intel(R) Xeon Phi(TM) CPU 7210 @ 1.30GHz
      1 "physical id"s (chips)
      256 "processors"
   cores, siblings (Caution: counting these is hw and system dependent.  The
   following excerpts from /proc/cpuinfo might not be reliable.  Use with
   caution.)
      cpu cores : 64
      siblings  : 256
      physical 0: cores 0 1 2 3 6 7 10 11 12 13 14 15 18 19 20 21 22 23 24 25 26
      27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51
      52 53 56 57 58 59 60 61 62 63 64 65 68 69 70 71 72 73
   cache size : 1024 KB

From /proc/meminfo
   MemTotal:       115193108 kB
   HugePages_Total:       0
   Hugepagesize:       2048 kB

/usr/bin/lsb_release -d
   CentOS Linux release 7.2.1511 (Core)

From /etc/*release* /etc/*version*
   centos-release: CentOS Linux release 7.2.1511 (Core)
   centos-release-upstream: Derived from Red Hat Enterprise Linux 7.2 (Source)
   os-release:
      NAME="CentOS Linux"
      VERSION="7 (Core)"
      ID="centos"
      ID_LIKE="rhel fedora"
      VERSION_ID="7"
      PRETTY_NAME="CentOS Linux 7 (Core)"
      ANSI_COLOR="0;31"
      CPE_NAME="cpe:/o:centos:centos:7"
   redhat-release: CentOS Linux release 7.2.1511 (Core)
   system-release: CentOS Linux release 7.2.1511 (Core)
   system-release-cpe: cpe:/o:centos:centos:7

uname -a:
   Linux knl1.uits.indiana.edu 3.10.0-327.13.1.el7.xppsl_1.3.3.151.x86_64 #1 SMP
   Fri Jun 10 15:04:35 UTC 2016 x86_64 x86_64 x86_64 GNU/Linux

run-level 3 May 2 10:51

SPEC is set to: /home/lijunj/spec/accel-test/75
   Filesystem     Type  Size  Used Avail Use% Mounted on
   /dev/sda3      ext4  713G  174G  503G  26% /

Cannot run dmidecode; consider saying 'chmod +s /usr/sbin/dmidecode'

(End of data from sysinfo program)
```

system config

General Notes

```
BIOS settings:
  Intel Simultaneous Multithreading (SMT): on
  Intel Turbo Boost Technology (Turbo)  : off
  Cluster Mode: quadrant
  Memory Mode: flat
  (MCDRAM is partitioned to the second NUMA node)

Current range for power measurement is 2.5A.
```

Base Compiler Invocation

C benchmarks:

icc

Fortran benchmarks:

ifort

Benchmarks using both Fortran and C:

icc ifort

Base Portability Flags

503.postencil: -DSPEC_USE_INNER_SIMD
504.polbm: -DSPEC_USE_INNER_SIMD
514.pomriq: -DSPEC_USE_INNER_SIMD
550.pmd: -DSPEC_USE_INNER_SIMD -80
551.ppalm: -DSPEC_USE_INNER_SIMD
552.pep: -DSPEC_USE_INNER_SIMD
553.pclvrleaf: -DSPEC_USE_INNER_SIMD
554.pcg: -DSPEC_USE_INNER_SIMD
555.pseismic: -DSPEC_USE_INNER_SIMD
556.psp: -DSPEC_USE_INNER_SIMD
557.pcsp: -DSPEC_U
559.pmniGhost: -DSPEC_U
560.pilbdc: -DSPEC_U
563.pswim: -DSPEC_USE_INNER_SIMD
570.pbt: -DSPEC_USE_INNER_SIMD

compiler switches

Base Optimization Flags

C benchmarks:

-O3 -qopenmp -qopenmp-offload=host -xMIC-AVX512

Fortran benchmarks:

-O3 -qopenmp -qopenmp-offload=host -xMIC-AVX512

Benchmarks using both Fortran and C:

-O3 -qopenmp -qopenmp-offload=host -xMIC-AVX512

The flags files that were used to format this result can be browsed at
https://www.spec.org/accel/flags/Intel-ic17.0-linux64.html,
https://www.spec.org/accel/flags/colfax-knl.html.

You can also download the XML flags sources by saving the following links:
https://www.spec.org/accel/flags/Intel-ic17.0-linux64.xml,
https://www.spec.org/accel/flags/colfax-knl.xml.

Reportable runs

Create valid/ compliant result for submission:

```
runspec --reportable [..]
```

- `--tune [base|all]`
- Entire SPEC suite (no single benchmarks)
- Workload: `test`, `train`, `ref` will be run → `ref` results are taken
  - Verification for all three data set sizes
- #iterations = 3 → median is taken for final reporting
- #threads: one fixed number in base (variable per benchmark in peak)

Configuration disclosure (in config file or with `rawformat`) → see next slide

Reportable run: https://www.spec.org/omp2012/Docs/runspec.html#section3.1.1
https://www.spec.org/omp2012/Docs/runspec.html#reportable

links

Output Files

- SPEC runs automatically generates:
- Benchmark reports: in txt, pdf, html formats
  - Preview of the result as it would look on the SPEC website
- Raw files, “.rsf”,
  - Editable fields includes system and software configuration
  - Non-editable fields: benchmark results are encrypted. Tampering with the results will corrupt the file.
- Log files, “.log”, “.log.debug”
  - Verbose output of the benchmark run

Submitting results to SPEC

- Submission of SPEC results
  1. Process your rsf-file through rawformat to check for anything missing/ faulty
  2. Attach your rsf-file to an e-mail to, e.g., subaccel@spec.org for Accel
  3. Receive a reply with a sub-file attached
  4. For updates, modify the sub-file and attach to an e-mail to, e.g., resubaccel@spec.org for Accel
- **Submitted results reviewed before publication by SPEC committee**
  - Schedule: 2 weeks review period before decision

Source: https://www.spec.org/accel/results/accel_acc.html

OpenACC (21):

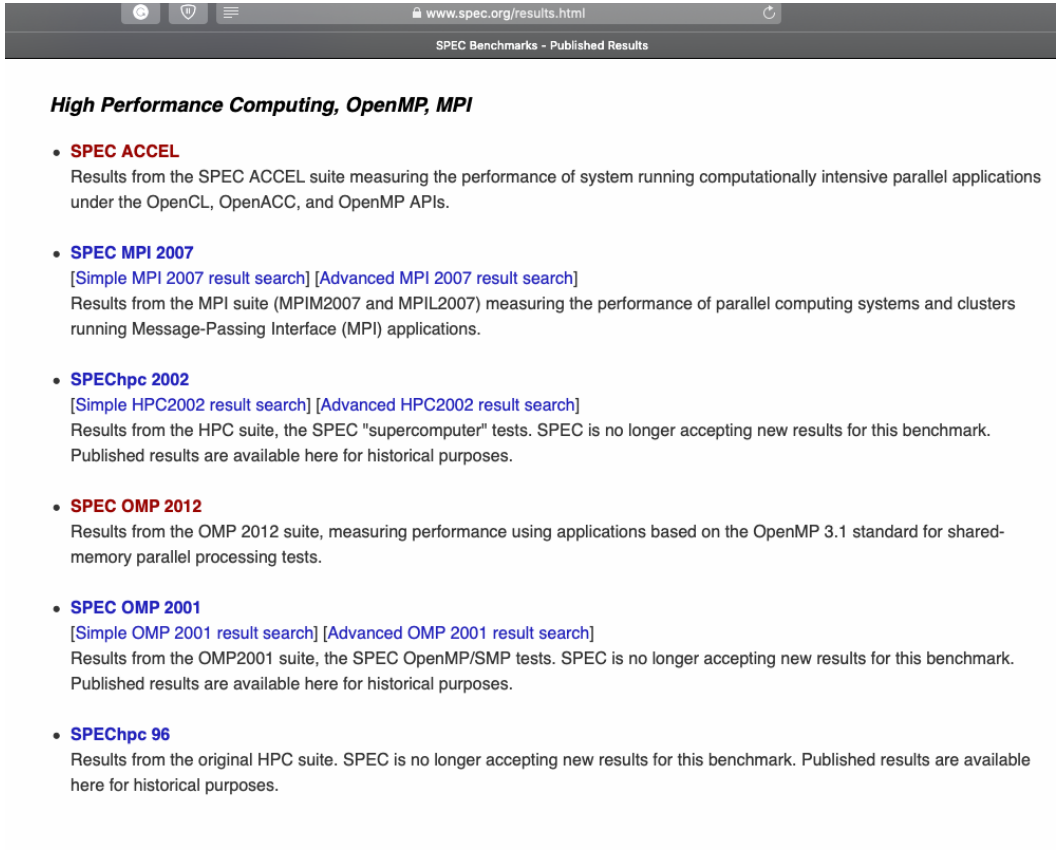
Test Sponsor	System Name	Accelerator Name	Results		Energy	
			Base	Peak	Base	Peak
Indiana University	Lenovo NeXtScale nx360 M5 HTML | CSV | Text | PDF | PS | Config	Intel Xeon E5-2680 v3	1.71	Not Run	--	--
Indiana University	HP Z820 Workstation HTML | CSV | Text | PDF | PS | Config	Intel Xeon E5-2640 v2	0.662	Not Run	1.10	--
Indiana University	Cray XC30 HTML | CSV | Text | PDF | PS | Config	Intel Xeon E5-2697 v2	1.18	Not Run	--	--
Indiana University	Cray XK7 HTML | CSV | Text | PDF | PS | Config	NVIDIA Tesla K20	1.71	Not Run	--	--
Indiana University	Cray XK7 HTML | CSV | Text | PDF | PS | Config	NVIDIA Tesla K20	1.78	Not Run	--	--
Indiana University	Cray XK7 HTML | CSV | Text | PDF | PS | Config	NVIDIA Tesla K20	2.00	Not Run	--	--
Indiana University	Cray XK7 HTML | CSV | Text | PDF | PS | Config	NVIDIA Tesla K20	2.01	Not Run	--	--
Indiana University	Cray XK7 HTML | CSV | Text | PDF | PS | Config	NVIDIA Tesla K20	2.07	Not Run	--	--
Lenovo Global Technology	ThinkSystem SR650 HTML | CSV | Text | PDF | PS | Config	NVIDIA Tesla V100-PCIE-16GB	12.2	Not Run	--	--
Lenovo Global Technology	ThinkSystem SR670 HTML | CSV | Text | PDF | PS | Config	Tesla V100-PCIE-16GB	12.0	Not Run	--	--
NVIDIA Corporation	SuperServer 1028GR-TR HTML | CSV | Text | PDF | PS | Config	Tesla K40m	2.56	2.56	--	--
NVIDIA Corporation	SuperServer 1028GR-TR HTML | CSV | Text | PDF | PS | Config	Intel Xeon E5-2698 v3	1.81	1.81	--	--
NVIDIA Corporation	SuperServer 1028GR-TR HTML | CSV | Text | PDF | PS | Config	Tesla P100-PCIE-16GB	8.02	8.02	--	--
Test Sponsor	**System Name**	**Accelerator Name**	**Results**		**Energy**	
			Base	**Peak**	**Base**	**Peak**
NVIDIA Corporation	SuperServer 1028GR-TR HTML | CSV | Text | PDF | PS | Config	Xeon E5-2698 v4	2.74	2.74	--	--
NVIDIA Corporation	A+ Server 1023US-TR4 HTML | CSV | Text | PDF | PS | Config	EPYC 7451	2.59	2.59	--	--
NVIDIA Corporation	SuperServer 1029GQ-TRT	Xeon Gold 6148	3.77	3.77	--	--

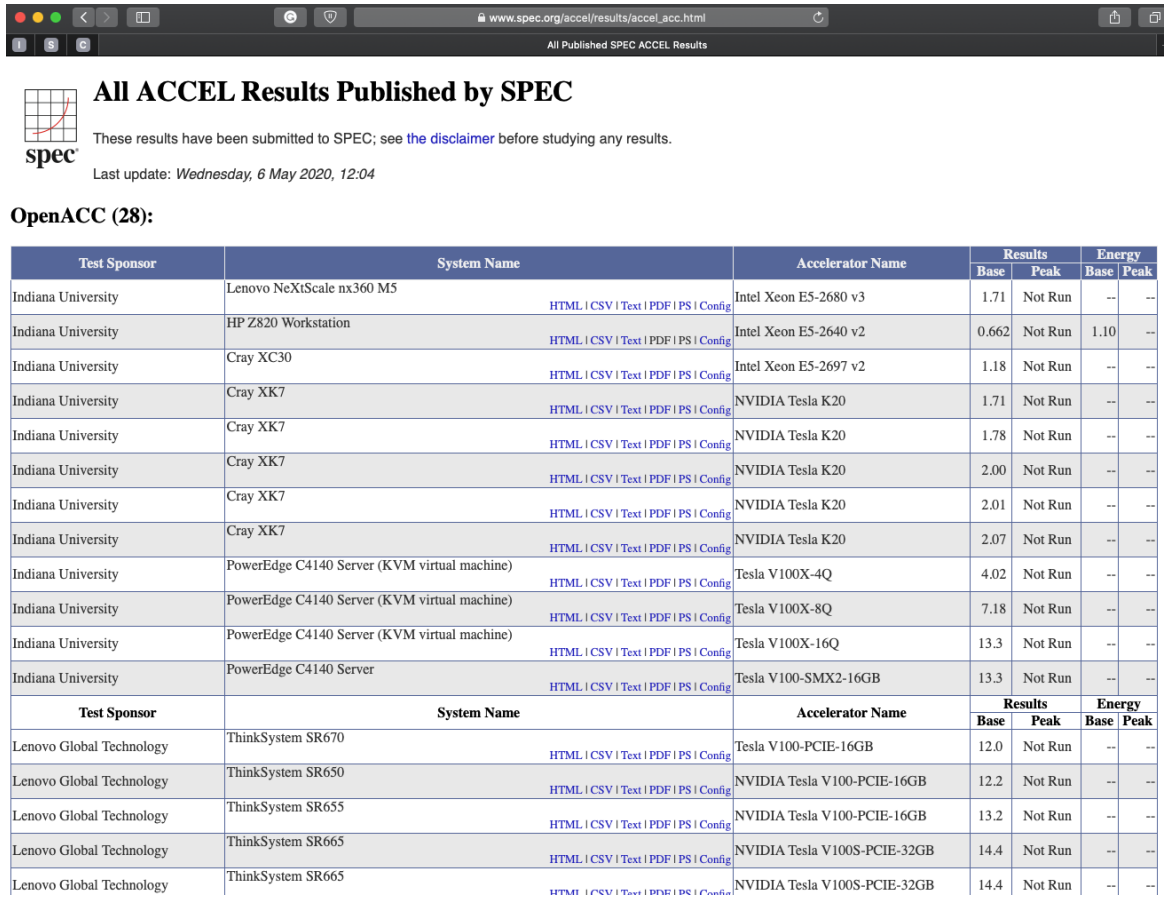
https://www.spec.org/accel/docs/runrules.html
https://www.spec.org/hpg/submitting_results.html

links

Result Disclosure

- All SPEC Official results are publicly available on SPEC website: https://www.spec.org/results.html
- Over 1400 published results, rich database for performance study





Test Sponsor	System Name	Accelerator Name	Results		Energy	
			Base	Peak	Base	Peak
Indiana University	Lenovo NeXtScale nx360 M5 HTML | CSV | Text | PDF | PS | Config	Intel Xeon E5-2680 v3	1.71	Not Run	--	--
Indiana University	HP Z820 Workstation HTML | CSV | Text | PDF | PS | Config	Intel Xeon E5-2640 v2	0.662	Not Run	1.10	--
Indiana University	Cray XC30 HTML | CSV | Text | PDF | PS | Config	Intel Xeon E5-2697 v2	1.18	Not Run	--	--
Indiana University	Cray XK7 HTML | CSV | Text | PDF | PS | Config	NVIDIA Tesla K20	1.71	Not Run	--	--
Indiana University	Cray XK7 HTML | CSV | Text | PDF | PS | Config	NVIDIA Tesla K20	1.78	Not Run	--	--
Indiana University	Cray XK7 HTML | CSV | Text | PDF | PS | Config	NVIDIA Tesla K20	2.00	Not Run	--	--
Indiana University	Cray XK7 HTML | CSV | Text | PDF | PS | Config	NVIDIA Tesla K20	2.01	Not Run	--	--
Indiana University	Cray XK7 HTML | CSV | Text | PDF | PS | Config	NVIDIA Tesla K20	2.07	Not Run	--	--
Indiana University	PowerEdge C4140 Server (KVM virtual machine) HTML | CSV | Text | PDF | PS | Config	Tesla V100X-4Q	4.02	Not Run	--	--
Indiana University	PowerEdge C4140 Server (KVM virtual machine) HTML | CSV | Text | PDF | PS | Config	Tesla V100X-8Q	7.18	Not Run	--	--
Indiana University	PowerEdge C4140 Server (KVM virtual machine) HTML | CSV | Text | PDF | PS | Config	Tesla V100X-16Q	13.3	Not Run	--	--
Indiana University	PowerEdge C4140 Server HTML | CSV | Text | PDF | PS | Config	Tesla V100-SMX2-16GB	13.3	Not Run	--	--
Test Sponsor	**System Name**	**Accelerator Name**	**Results**		**Energy**	
			Base	**Peak**	**Base**	**Peak**
Lenovo Global Technology	ThinkSystem SR670 HTML | CSV | Text | PDF | PS | Config	Tesla V100-PCIE-16GB	12.0	Not Run	--	--
Lenovo Global Technology	ThinkSystem SR650 HTML | CSV | Text | PDF | PS | Config	NVIDIA Tesla V100-PCIE-16GB	12.2	Not Run	--	--
Lenovo Global Technology	ThinkSystem SR655 HTML | CSV | Text | PDF | PS | Config	NVIDIA Tesla V100-PCIE-16GB	13.2	Not Run	--	--
Lenovo Global Technology	ThinkSystem SR665 HTML | CSV | Text | PDF | PS | Config	NVIDIA Tesla V100S-PCIE-32GB	14.4	Not Run	--	--
Lenovo Global Technology	ThinkSystem SR665 HTML | CSV | Text | PDF | PS | Config	NVIDIA Tesla V100S-PCIE-32GB	14.4	Not Run	--	--

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SPEC can go after any misuse (under license agreement).
A few recent cases:

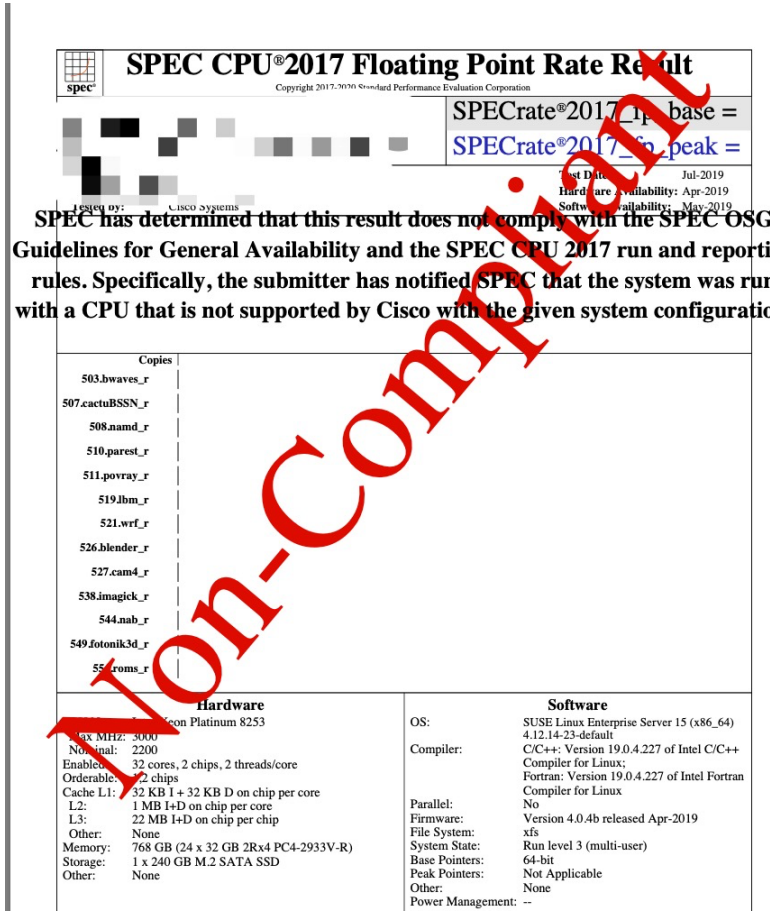
- (osgmail-54973) Mar-2020, CPU maker A found CPU maker B claimed “36% more performance” than previous gen product using SPEC benchmarks.
  - no basis of comparison or how the speedup was calculated
  - no SPEC official metric was used
  - unpublished SPEC results need to be marked as “estimate”
  - company B eventually changed their press release with SPEC suggested changes.

- (osgmail-54450) Dec-2019. It’s found production machine from vendor X has different software/hardware setup, the performance was not reproducible. Their 12 published results were marked non-compliant with score remoted.

- (osgmail-51786) Jan-2019. Company C who was a relatively new member released new chip claiming certain SPEC score without submitting report to SPEC for review.
  - Company C was made to modify their press release with clear mark that the score was unofficial estimate.

- (osgmail-50759) Jun-2018. Vendor Y acquired machine made by vendor Z, and found they cannot achieve the same performance as their published results. 4 results were sent back for re-review.

- ……


SPEC CPU®2017 Floating Point Rate Result

SPECrate®2017_fp_base =

SPECrate®2017_fp_peak =

Test Date: Jul-2019

Hardware Availability: Apr-2019

Software Availability: May-2019

Tested by: Cisco Systems

SPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reportin rules. Specifically, the submitter has notified SPEC that the system was run with a CPU that is not supported by Cisco with the given system configuration

Copies

503.bwaves_r

507.cactuBSSN_r

508.namd_r

510.parest_r

511.povray_r

519.lbm_r

521.wrf_r

526.blender_r

527.cam4_r

538.imagick_r

544.nab_r

549.fotonik3d_r

55[illegible]roms_r

Hardware

[illegible]con Platinum 8253

Max MHz: 3000

Nominal: 2200

Enabled: 32 cores, 2 chips, 2 threads/core

Orderable: 2 chips

Cache L1: 32 KB I + 32 KB D on chip per core

L2: 1 MB I+D on chip per core

L3: 22 MB I+D on chip per chip

Other: None

Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)

Storage: 1 x 240 GB M.2 SATA SSD

Other: None

Software

OS: SUSE Linux Enterprise Server 15 (x86_64) 4.12.14-23-default

Compiler: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux; Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux

Parallel: No

Firmware: Version 4.0.4b released Apr-2019

File System: xfs

System State: Run level 3 (multi-user)

Base Pointers: 64-bit

Peak Pointers: Not Applicable

Other: None

Power Management: --

Non-Compliant

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3. Diagrams, Tables, and Abstracts must have sufficient context on their own so that they are not misleading as to compliance.
4. If non-compliant numbers are compared to compliant results it must be clear from the context which is which.

Summary of SPEC Benchmark Philosophy

- SPEC benchmarks includes real applications
- SPEC tools maintenances consistency of the runs and check correctness
- SPEC score is speedup comparing to a reference machine, higher is better
- Each benchmark has its run rule
- All performance related aspects need to be documented in the report for reproducibility
- All results submitted to SPEC for publication will go through 2-week peer-review
- Feel free to use SPEC benchmarks for your research, just mark your result as “estimate” if it is not compliant with run rule

Contents

I. SPEC benchmark philosophy

a) Structure of SPEC benchmarks
- components & workloads & tools
- SPEC score
- brief story of run rules
- Configuration files
- From base to peak runs

b) Result Disclosure
- Documentation and benchmark report
- Reportable runs
- the peer-review process for publishing

II. Use SPEC benchmarks for decision making
- procurement process
- test performance of compilers
- compiler validation
- explore performance of new architectures

III. Benchmark acquisition & licensing
- commercial license
- academic license
- become a member

Use SPEC benchmarks for decision making:
procurement process

RFP

- all major HPC vendors are SPEC members
- they are all familiar with SPEC benchmarks
- easier for vendors to provide you SPEC results than testing your customized application
- application benchmark gives a better correlation to the real life performance
- SPEC peer-review process guarantees fairness

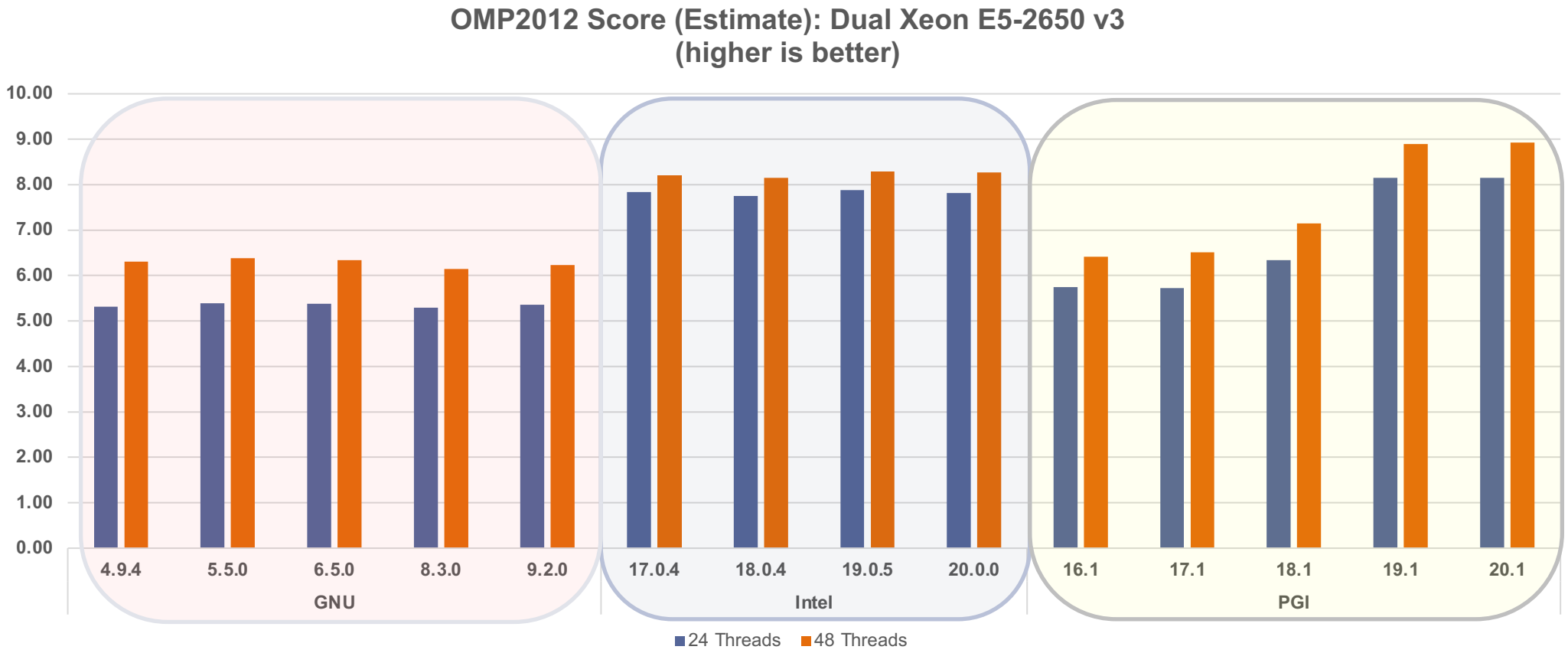
Acceptance Test

- make sure real applications work well
- compare performance with published SPEC results
- test and find optimal software stack (default compiler, default MPI, etc.)

Use SPEC benchmarks for decision making:
test performance of compilers

Compiler Performance on OMP2012

- no improvement for GNU
- consistent high performance for Intel (especially for Fortran)
- descent improvement over 5 years for PGI (major improvement in Fortran)



Use SPEC benchmarks for decision making:
test performance of compilers

Compiler Validation

- GNU OpenACC support under development
- SPEC Accel OpenACC benchmark being used by IU, ORNL, GNU/Mentor Graphics

SPEC **Estimated** Scores on V100

benchmark name	GCC/8.1.1 ACC branch *	PGI/18.4
303.ostencil	2.38	13.3
304.olbm	**13.6**	**11.3**
314.omriq	2.76	19.0
360.ilbdc	7.55	10.1
Total Score (all 15 codes)	0.40	9.96

- With come hacks, GCC compiles all 15 benchmarks
- GCC currently will run ”acc kernels” serially on CPU.
- GCC handles “acc parallel” well.
- 4 out of 15 ACC benchmarks do not use “acc kernels”

* Info about GCC OpenACC branch: https://gcc.gnu.org/wiki/OpenACC

Use SPEC benchmarks for decision making:

Compare performance of different architectures

GPU vs KNL, which worth investment?

- SPEC Accel OpenACC and OpenMP have same workload, same serial code, different directives
- based on runtime from in-house test data, published SPEC data and estimate from core/freq

OpenMP 4.5 (Intel 17)

estimate 6.4 x Xeon Phi 7290 (KNL) MSRP $6,254

5.6 x Xeon Phi 7250 (KNL) MSRP $4,876

4.7 x 2x Xeon E5-2697 v4 MSRP $5,404

4.6 x Xeon Phi 7210 (KNL) MSRP $2,438

3.1x 2x Xeon E5-2680 v3

2.4x 2x Xeon E5-2697 v2

1.4 x 2x Xeon E5-2640 v2

1.3 x Xeon Phi 5110p (KNC)

OpenACC (PGI 17)

Tesla P100 12.4x MSRP $8,000

Tesla K40m 3.9x $2,200

Tesla K20x 3.4x

2x Xeon E5-2680 v3 2.6x

2x Xeon E5-2697 v2 1.8x

2x Xeon E5-2640 v2 **1.0x ***

derived speedup based on runtime in SPEC Accel OMP and SPEC Accel ACC

* Use dual Xeon E5-2640 v2 OpenACC as baseline

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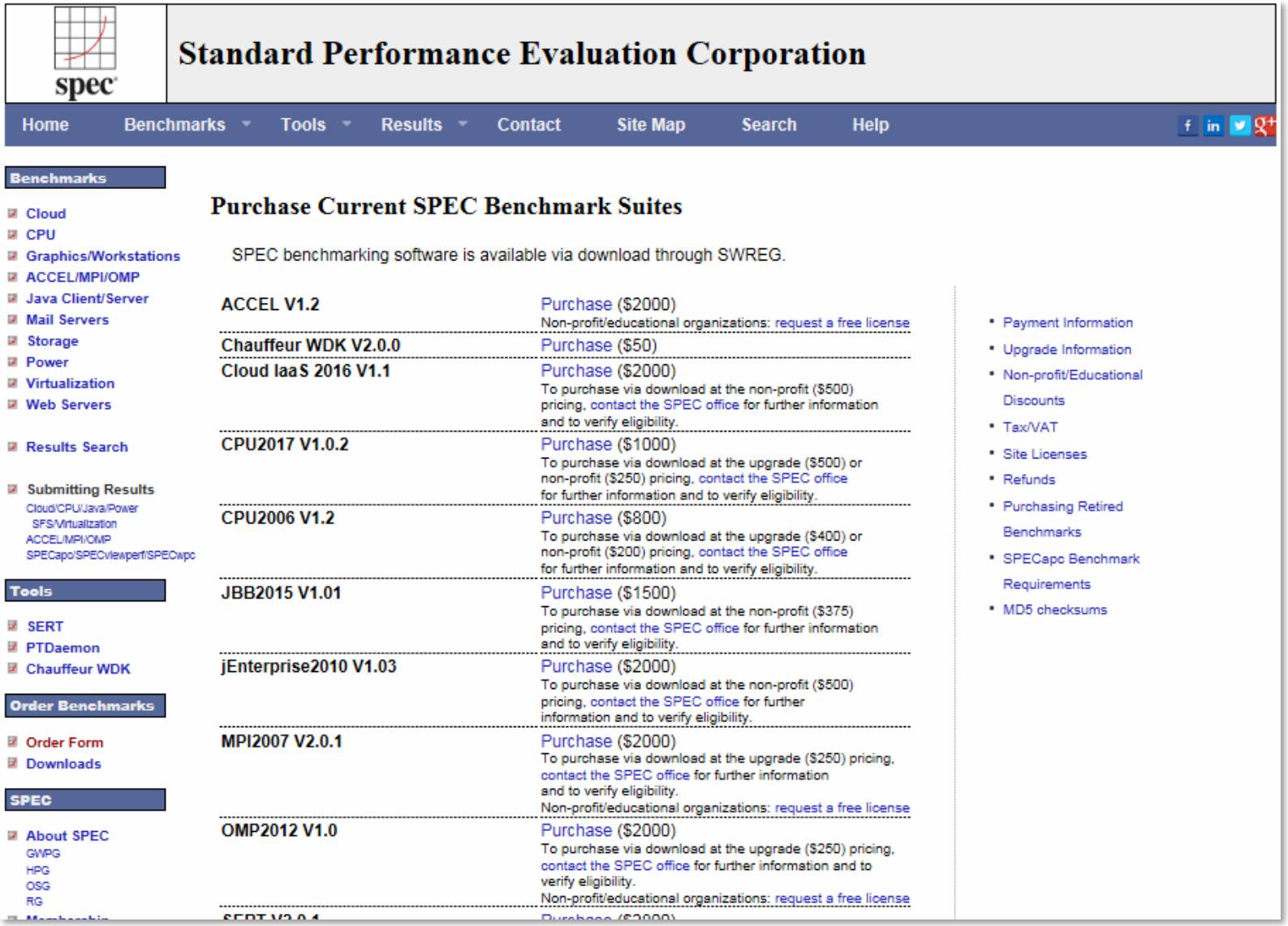
Acquisition of SPEC Benchmarks



http://spec.org/order.html
https://www.spec.org/hpg/joining.html

links

- Single SPEC suites
  - Commercial license
  - Non-profit license
- SPEC membership
  - Receive benchmarks for free

Acquisition of SPEC Benchmarks

Press Release 2018: https://www.spec.org/news/hpgnonprofitpricing.html

Non-commercial download + definition:
http://spec.org/hpgdownload.html

links

- Commercial license
  - Must be purchased via order form
  - Commercial enterprises (not being SPEC/HPG member) engaging in marketing, developing, testing, consulting for and/or selling computers, computer services, accelerator devices, drivers, software or other high performance computing systems or components in the computer marketplace
- Non-commercial license
  - Free of charge
  - Organizations that do not require a commercial license
  - Valid for the organization (not individual)
  - Institutional e-mail address required

Benchmark Suite	Non-Profit	Commercial
CPU2017 V1.0.2	$250	$1,000
ACCEL V1.3	free	$2,000
OMP2012 V1.0	free	$2,000
MPI2007 V2.0.1	free	$2,000
SPECpower_ssj2008 V1.12	$400	$1,600

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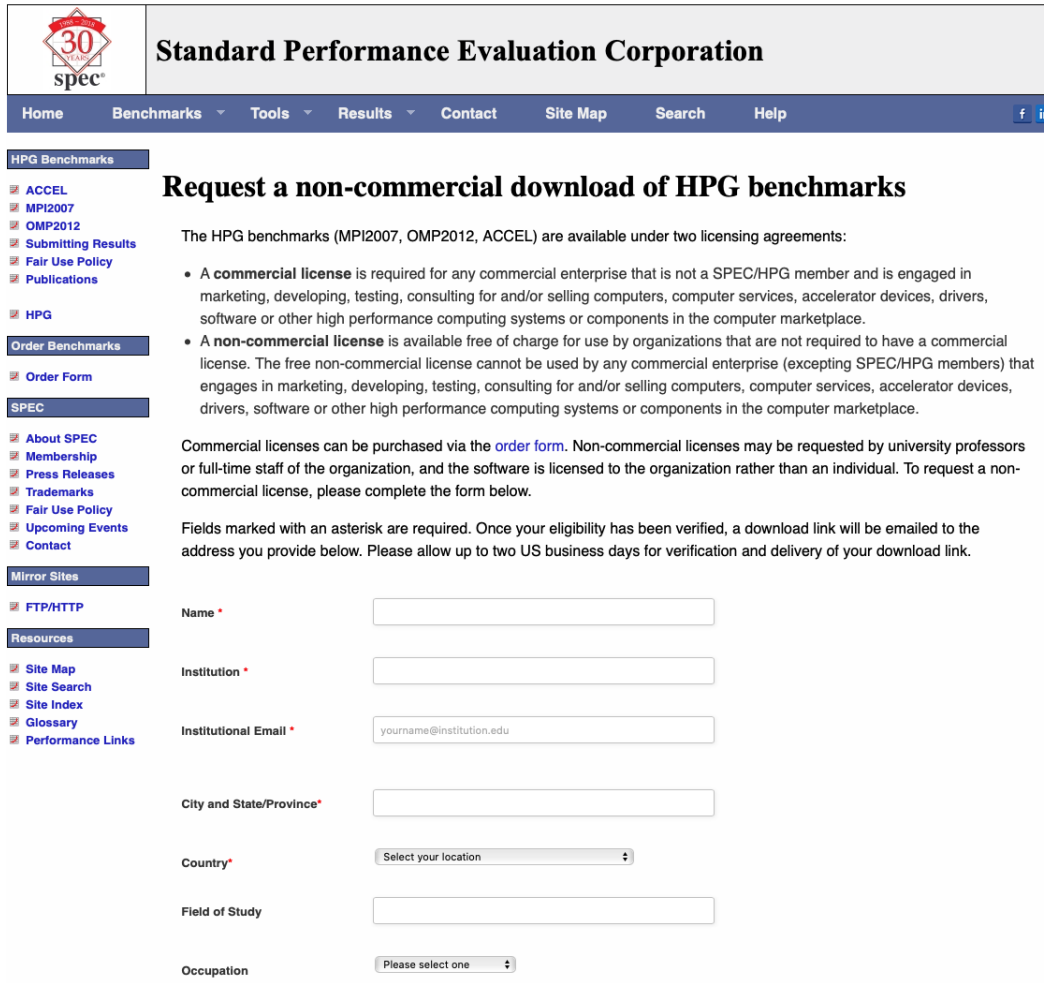
Free Non-commercial download + definition: http://spec.org/hpgdownload.html



Standard Performance Evaluation Corporation

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HPG Benchmarks
- ACCEL
- MPI2007
- OMP2012
- Submitting Results
- Fair Use Policy
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- Trademarks
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- Upcoming Events
- Contact

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- FTP/HTTP

Resources
- Site Map
- Site Search
- Site Index
- Glossary
- Performance Links

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Institution *

Institutional Email * yourname@institution.edu

City and State/Province*

Country* Select your location

Field of Study

Occupation Please select one

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  - research labs, universities, government org, etc.
  - as simple as filling out a lightweight form
  - provide your institutional email for verification
  - SPEC office will check your eligibility and send you the download link

- **As of Q3-2020, 270 institutions have requested and been granted free license.**

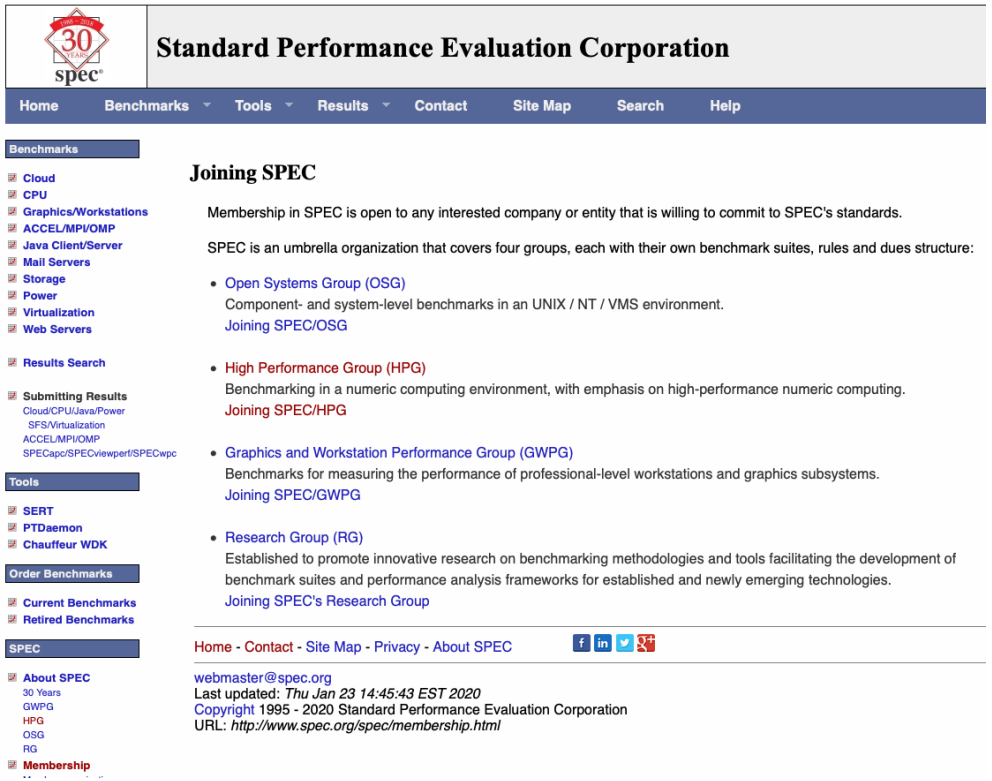
  (multiple requests from the same institute counts as one)

Become a Member

Become a member

- get access to all the benchmarks for free
- connect with all chip makers, vendors, compiler developers, universities, national labs, etc.…
- learn the last development in software and hardware
- join the team work creating future benchmarks

- commercial member: $8000/y (more voting rights)
- academic member: $800/y
- https://www.spec.org/spec/membership.html
- please inquiry the SPEC office: info@spec.org



Thank you!

Questions?

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