8335-GTB Hardware Architecture Overview

Chris Mann
Power Systems Development
January 6, 2017

Garrison Architecture Overview - Agenda

- Hardware Overview
- Processor Interfaces
- Memory Architecture
- GPU Interconnect
- I/O Interconnect

Garrison Architecture Overview - Agenda

- Hardware Overview
- Processor Interfaces
- Memory Architecture
- GPU Interconnect
- I/O Interconnect

3

Garrison Design - 2 Socket P8 with NVLink, 4 GPU System

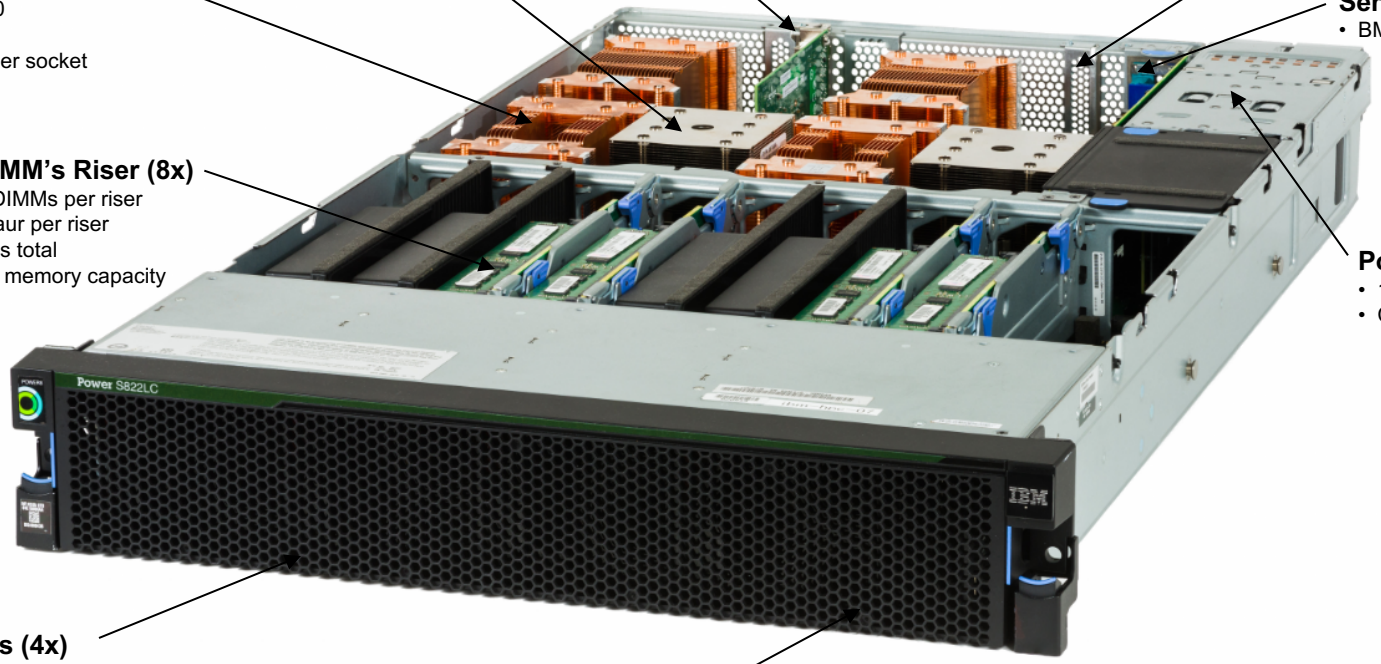
Power 8 with NVLink (2x)
- 190W Sort
- Integrated NVLink 1.0

PCIe slot (2x)
- Gen3 PCIe
- HHHL Adapter

PCIe slot (1x)
- Gen3 PCIe
- HHHL Adapter

NVidia GPU
- SXM2 form factor
- NVLink 1.0
- 300 W
- Max of 2 per socket

Service Controller Card
- BMC Content



Memory DIMM's Riser (8x)
- 4 IS DDR4 DIMMs per riser
- Single Centaur per riser
- 32 IS DIMM's total
- 32-1024 GB memory capacity

Power Supplies (2x)
- 1300W
- Common Form Factor Supply

Cooling Fans (4x)
- 80mm Counter- Rotating Fans
- Hot swap

Storage Option (2x)
- 0-2, SATA HDD.SSD
- Tray design for install/removal
- Hot Swap

Garrison Design - 2 Socket P8 with NVLink, 4 GPU System

Power Supplies (2x)
- 1300W
- Common Form Factor Supply

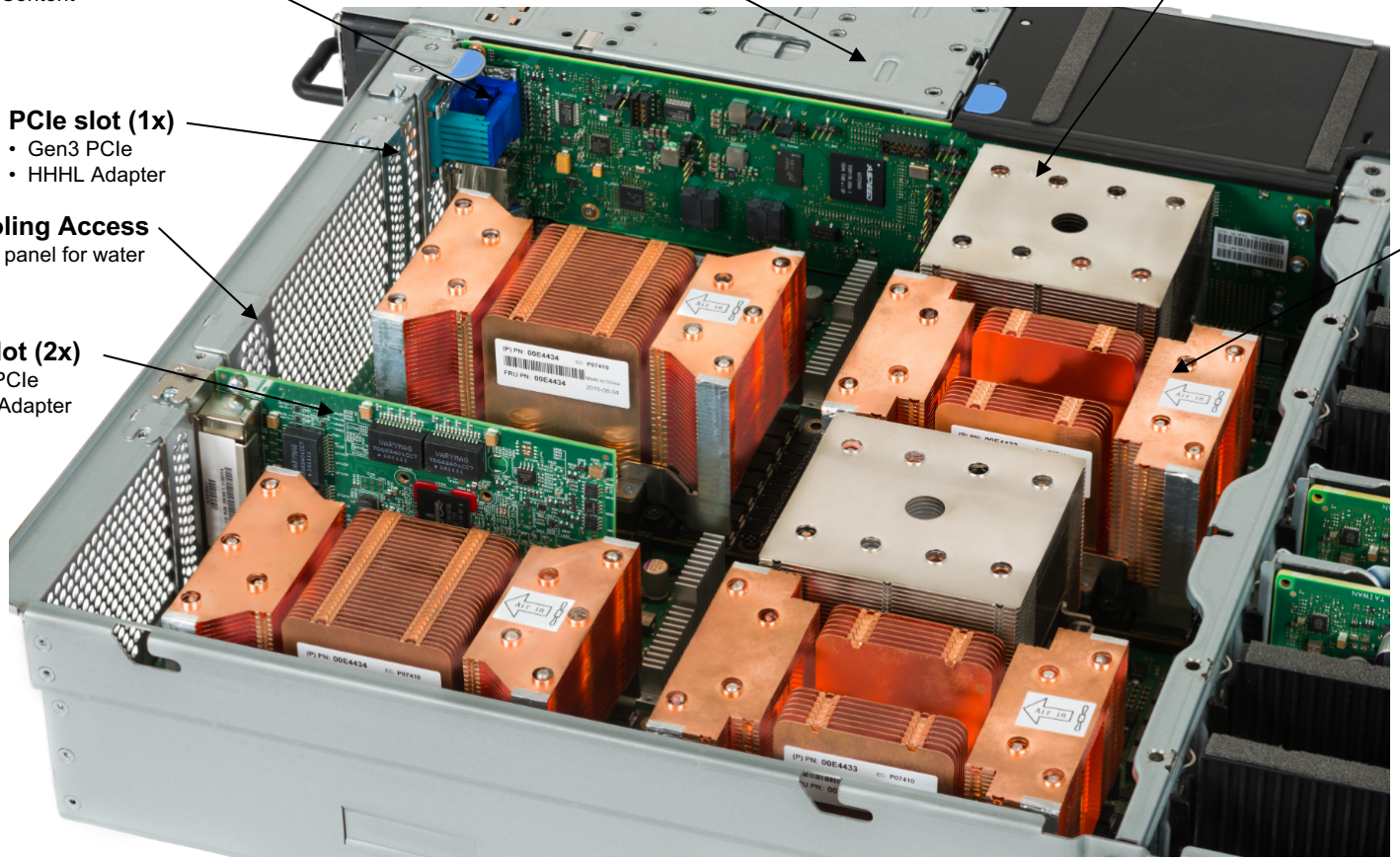
Power 8 with NVLink (2x)
- 190W Sort
- Integrated NVLink 1.0

Service Controller Card
- BMC Content

PCIe slot (1x)
- Gen3 PCIe
- HHHL Adapter

Water Cooling Access
- Removable panel for water line access

PCIe slot (2x)
- Gen3 PCIe
- HHHL Adapter



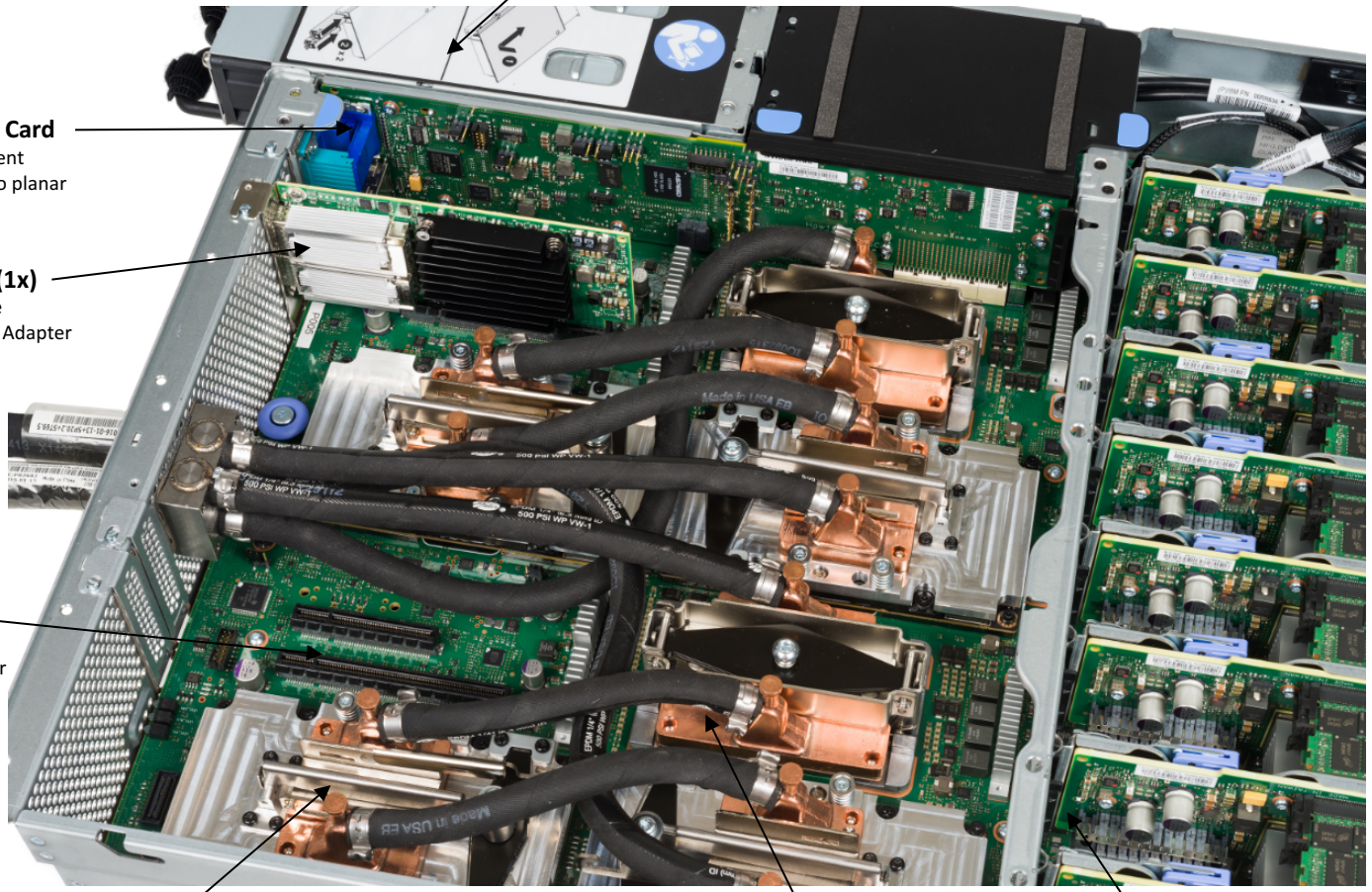
NVidia GPU
- SXM2 form factor
- NVLink 1.0
- 300 W
- Max of 2 per socket

Garrison Design – Water Cooled 2 Socket P8 with NVLink, 4 GPU Server

Power Supplies (2x)
- 1300W
- Common Form Factor Supply

Service Controller Card
- Firestone BMC Content
- Daughter card due to planar space constraints

PCIe slot (1x)
- Gen3 PCIe
- x16 HHHL Adapter



PCIe slot (2x)
- Gen3 PCIe
- 1, x16 HHHL Adapter
- 1, x8 HHHL Adapter

NVidia GPU (4x)
- SXM2 form factor
- NVLink 1.0
- 300 W
- 2 per socket

Power 8 with NVLink (2x)
- 190W Sort
- Integrated NVLink 1.0

Memory DIMM's Riser (8x)
- 4 IS DDR4 DIMMs per Riser
- Single Centaur per Riser
- 32 IS DIMM's total

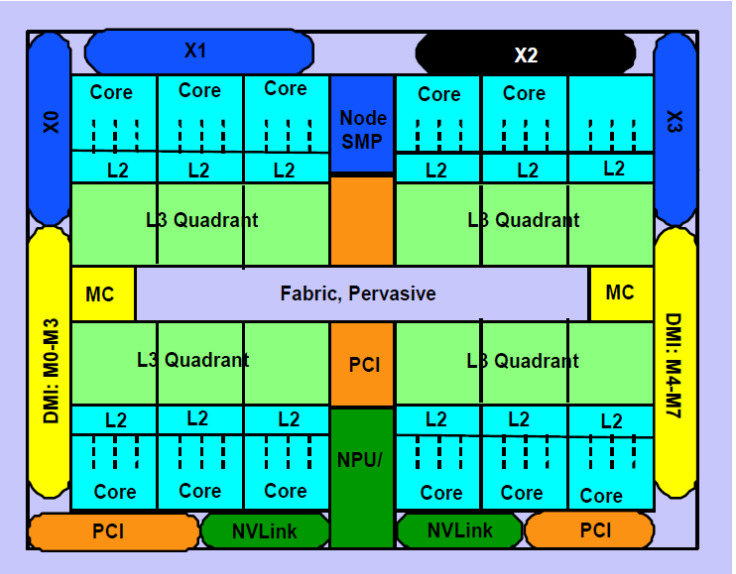
Garrison Architecture Overview - Agenda

- Hardware Overview
- Processor Interfaces
- Memory Architecture
- GPU Interconnect
- I/O Interconnect

7

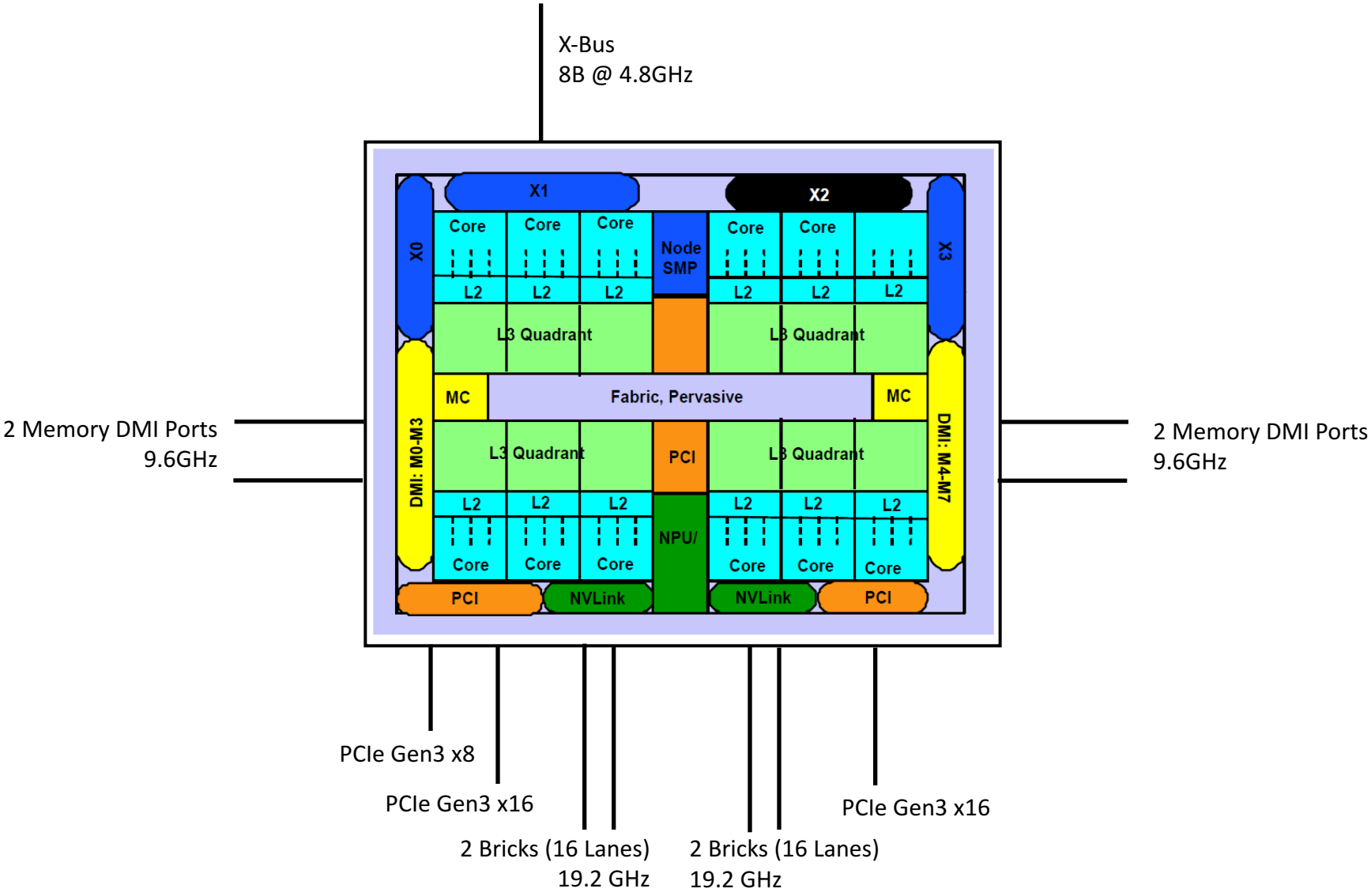
POWER8 with NVLink Overview

- Processor Chip
  - 659mm2, 22nm SOI with embedded DRAM
- 12 Processor core per chip
  - Up to 8 threads per core (SMT8)
  - 4 Concurrent LPARs per core
  - Garrison uses 8, 10 Core sorts
- Integrated SMP interconnect
  - Single 8B X-B bus at 4.8GHz
- Integrated Memory Controller
  - 4 High Speed DMI ports at 9.6GHz
  - 16MB memory cache / buffer chip (Centaur)
- GPU Interfaces
  - 4 Bricks (32 lanes) NVLink 1.0
  - Each brick running at 19.2GB/s
- Integrated I/O Sub-system
  - 40 PCIe Gen 3 lanes
  - 2, x16 and 1, x8 interfaces
  - Support for 2 CAPI connections over the x16 PCIe
- Fine Grained Power Management
  - On chip controller, Power gating and on chip VRM



	Frequency	TDP Power	Frequency	TDP $T_{j\ core\ avg}$	RDP Power	RDP $T_{j\ core\ avg}$
10 Core, 100% CLY	2.860 GHz	190W	3.492 GHz	70C	252W	85C
8 Core, 100% CLY	3.259 GHz	190W	3.857 GHz	70C	260W	85C

POWER8 with NVLink Module Interfaces

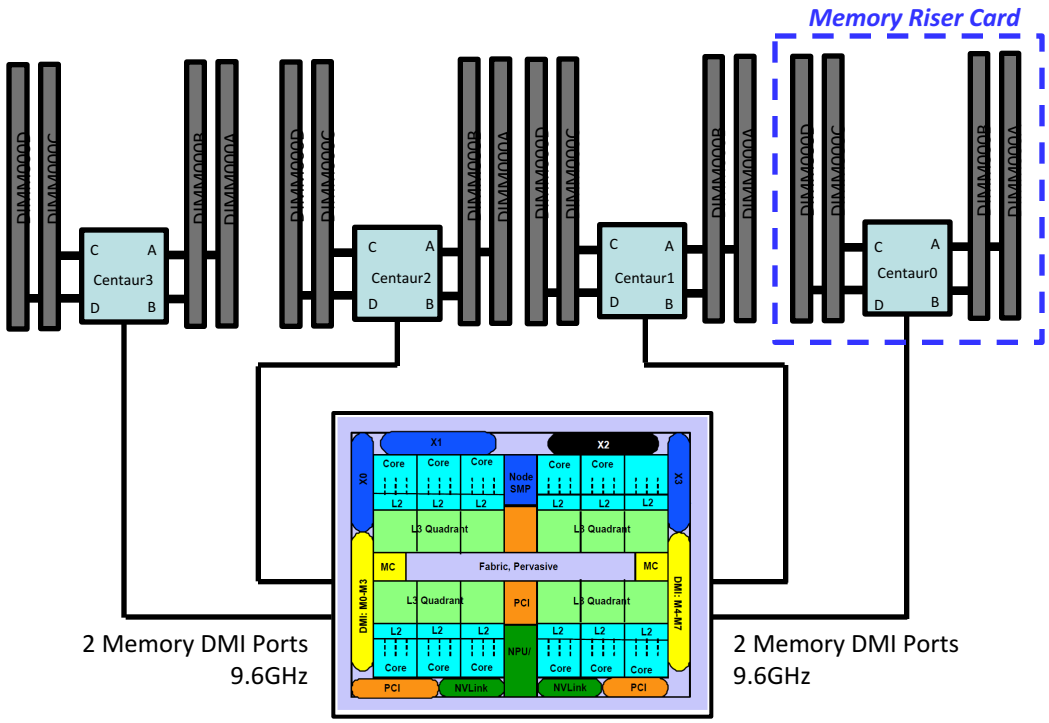


Garrison Architecture Overview - Agenda

- Hardware Overview
- Processor Interfaces
- Memory Architecture
- GPU Interconnect
- I/O Interconnect

Garrison Memory Interconnect Summary

- DMI Interface
  - Unidirectional interface to allow for high frequency and high effective data rates
- Memory Controller in Buffer
  - 2 Memory controllers located in buffer chip, each controlling 2, 8 byte interfaces to the memory DIMMs
- 115GB/second Peak DMI Bandwidth
  - 3 bytes x 4 channels x 9.6 Gbits/sec
- 205 GB/second Peak Memory Bandwidth
  - 32 bytes x 4 buffers x 1.6 Gb/s data rate
- Industry Standard DIMMs
  - 4, 8, 16 and 32GB DIMMs
  - 128 – 1024 GB system capacity

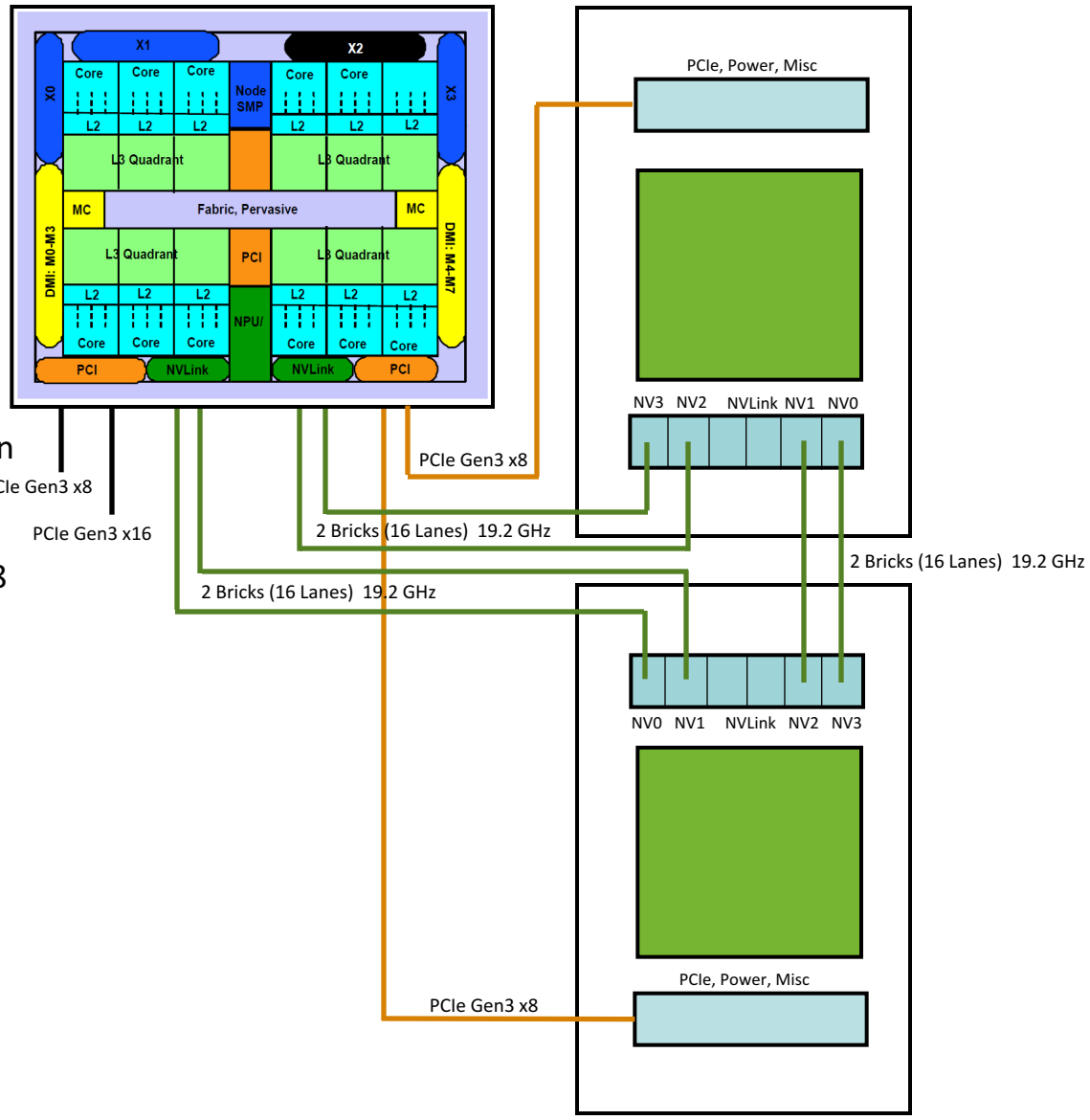


Garrison Architecture Overview - Agenda

- Hardware Overview
- Processor Interfaces
- Memory Architecture
- GPU Interconnect
- I/O Interconnect

GPU Interconnect

- NVLink Interface
  - High bandwidth interface far exceeding any existing or planned future PCIe interface
  - 16 Lanes CPU to GPU
  - 16 Lanes GPU to GPU
- PCIe Interface
  - Used for initiation, control and in band reporting of GPU status
  - PCIe x16 interface on the GPU, Garrison uses this interface in x8 mode

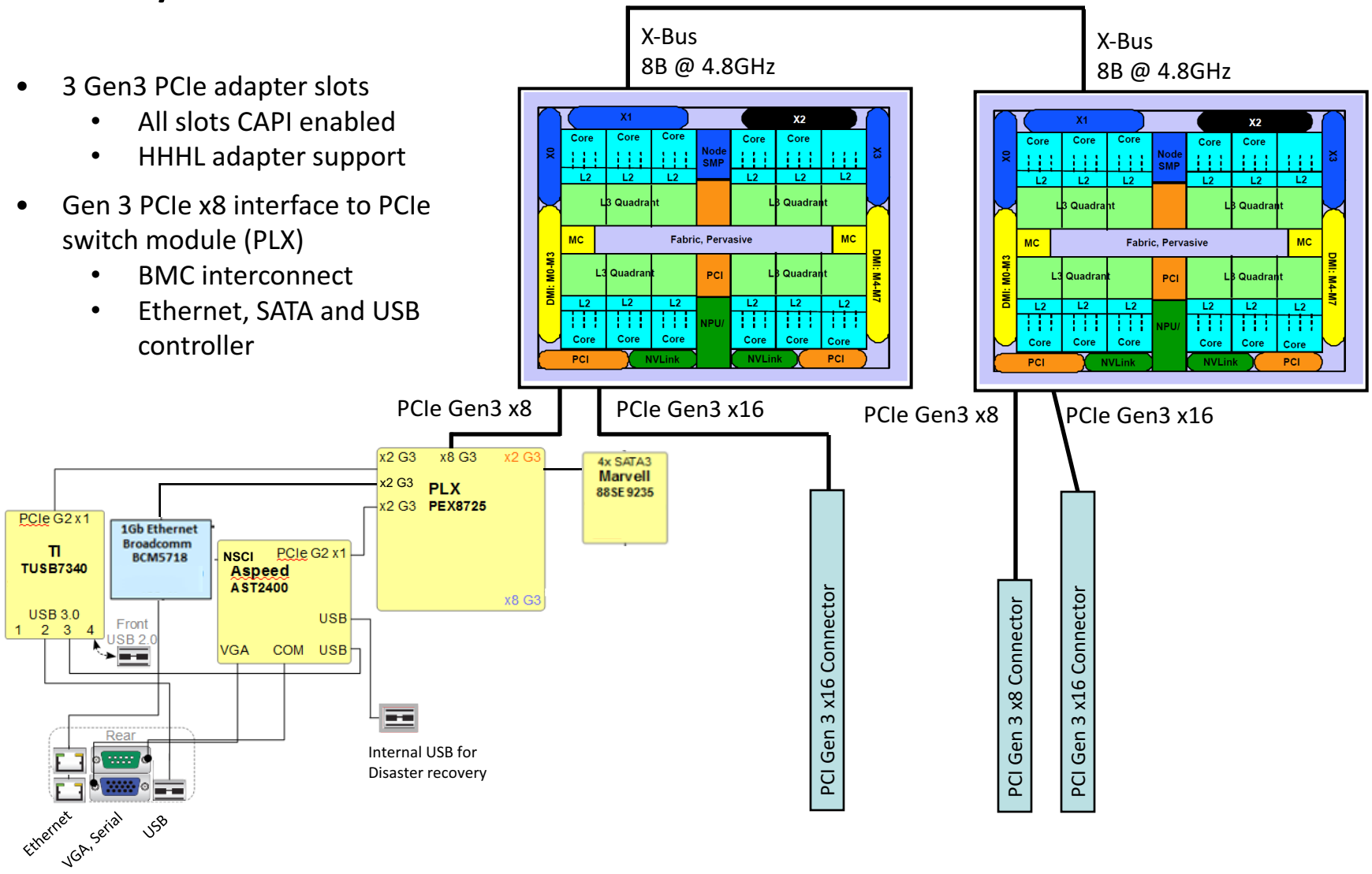


Garrison Architecture Overview - Agenda

- Hardware Overview
- Processor Interfaces
- Memory Architecture
- GPU Interconnect
- I/O Interconnect

Garrison I/O Interconnect

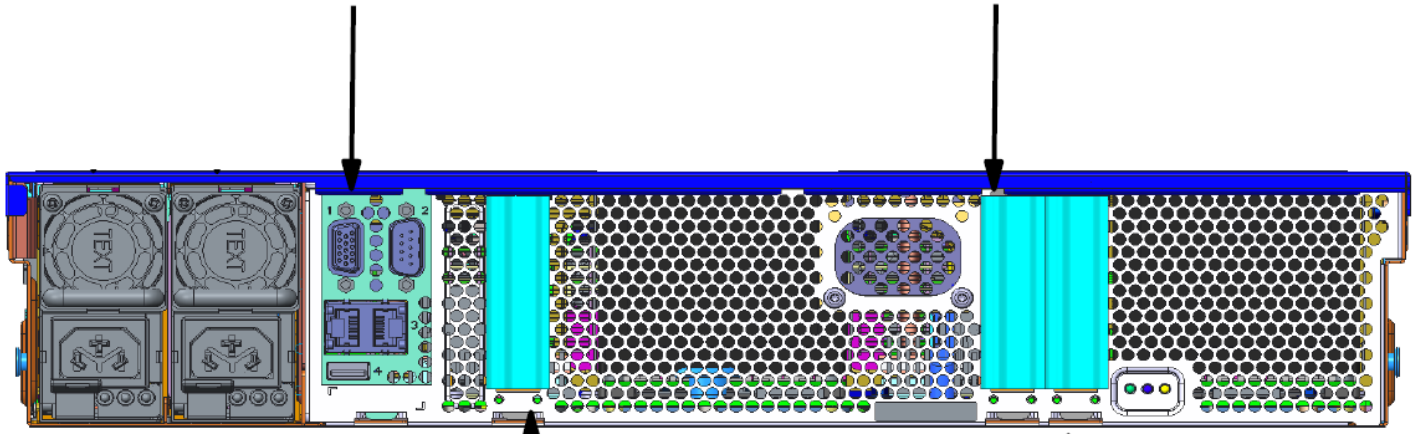
- 3 Gen3 PCIe adapter slots
  - All slots CAPI enabled
  - HHHL adapter support
- Gen 3 PCIe x8 interface to PCIe switch module (PLX)
  - BMC interconnect
  - Ethernet, SATA and USB controller



Garrison I/O Interconnect

Hawthorn
- Gb Ethernet
- USB3.0
- Management

PCIe Slot 2
- Gen3 x8
- CAPI enabled

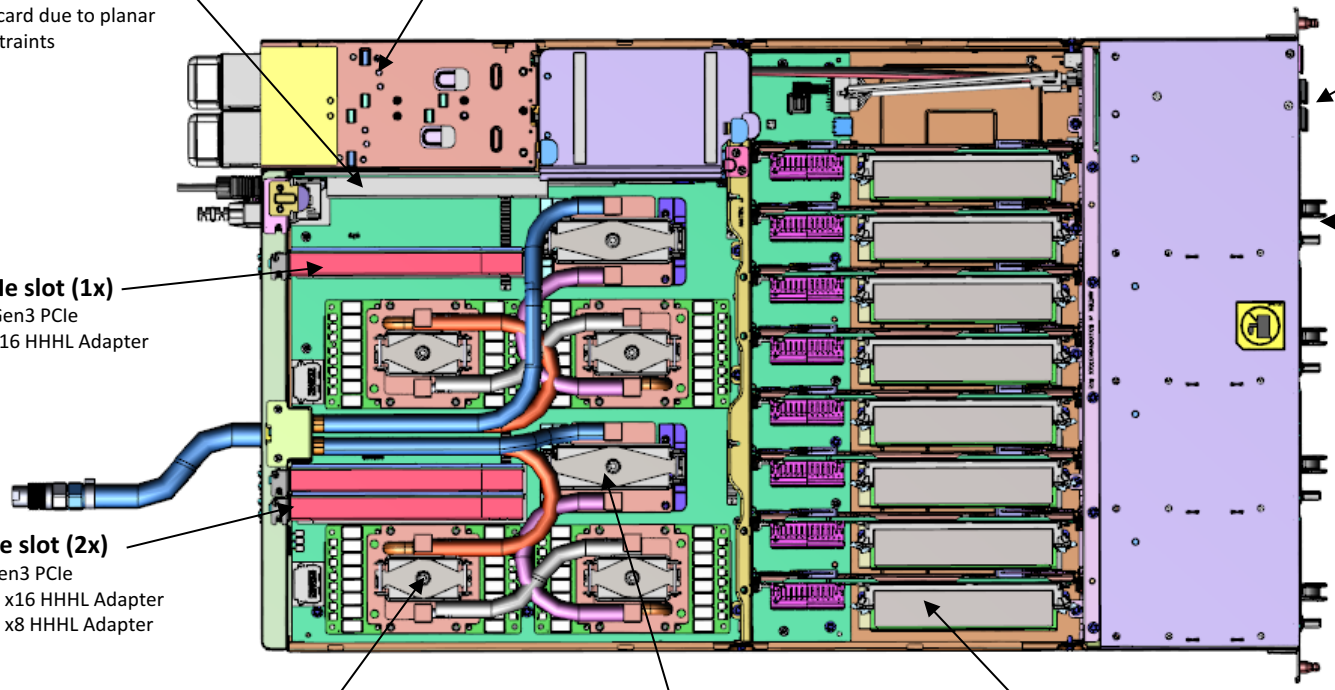


PCIe Slot 1
- Gen3 x16
- CAPI enabled

PCIe Slot 3
- Gen3 x16
- CAPI enabled

Backup

Garrison Concept – Water Cooled 2 Socket P8 with NVLink, 4 GPU Server



Power Supplies (2x)
- 1300W
- Configuration limits for redundancy
- Hot Swap
- Common Form Factor Supply

Service Controller Card
- Firestone BMC Content
- Daughter card due to planar space constraints

HDD Option (2x)
- Tray design for install/removal
- Hot Swap
- Front Service
- Replaces fan module

Cooling Fans (4x)
- 80mm Counter- Rotating Fans
- Hot swap

PCIe slot (1x)
- Gen3 PCIe
- x16 HHHL Adapter

PCIe slot (2x)
- Gen3 PCIe
- 1, x16 HHHL Adapter
- 1, x8 HHHL Adapter

NVidia GPU (2/4x)
- SXM2 form factor
- NVLink 1.0
- 300 W
- 1-2 per socket

Power 8 with NVLink (2x)
- 190W Sort
- Integrated NVLink 1.0

Memory DIMM's Riser (8x)
- 4 IS DDR4 DIMMs per Riser
- Single Centaur per Riser
- 32 IS DIMM's total

Garrison Memory Interconnect