Application Requirements for Next-Generation OLCF Systems

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OLCF 2024 Roadmap

We have increased our systems capability at our center since 2004 by a factor of 10,000X

We are currently at 27PF, however the Exascale reports have pointed out that systems will be required at the level of 1 EF and beyond in order to reach critical DOE science goals

Our facilities plan therefore is to deploy a system of up to 4 EF capability by 2024

Our next step is the OLCF-4 "CORAL" system at 100-200PF to be deployed in the 2017-2018 timeframe

Application Requirements

DOE Agency Priority Goal: "Identify programmatic drivers and technical requirements in coordination with other Departmental mission areas to inform future development of high performance computing capabilities and in anticipation of capable exascale systems ." (*DOE Strategic Plan 2014- 2018*)

To help us understand the compute capabilities needed for future systems from the standpoint of applications, we periodically go through an applications requirements process

https://www.olcf.ornl.gov/mediacenter/center-reports

INSTIGUEL Laborators

The Requirements Process

- We take input from multiple sources:
	- DOE science mandates
	- OLCF Leadership Computing usage statistics for the recent past to understand how users are using our systems
	- A requirements survey to elicit project requirements from OLCF-supported projects
	- Discussions with computer hardware and software vendors on capabilities of nextgeneration offerings
- We seek to understand items/specifications needed in order for science teams to meet their science objectives, for example:

system hardware requirements science model requirements system software requirements algorithm requirements compilers, libraries, tools application codes data storage, access, analysis development processes workflow management

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1. OLCF System Usage

System logs tell us the demand to run large jobs continues to be high and growing

The "leadership metric": what fraction of our corehours are used in jobs requiring >20% of the full system

The average for Titan has been 62% YTD

Up from 43% for JaguarPF over its lifetime

Titan GPU Usage

Many projects are making effective use of accelerated heterogeneous nodes on Titan

We are improving our tools for tracking GPU usage

Usage is substantial and

Assessing GPU Usage with ALTD

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Average Job Size - JaguarPF

Users need to be able to run jobs of all sizes

Cumulative graph shows the distribution of how core-hours are used with respect to job size

Average Job Duration - JaguarPF

Users have learned how to limit their job sizes, using e.g. checkpoint/restart when necessary

Cumulative graph showing the distribution of how core-hours are used with respect to job duration

88% of core-hours spent on jobs < 12 hours

Half of core-hours spent on jobs of < 6 hours

Algorithmic Motifs

Top-used codes span the whole range of algorithmic motifs

2. 2013 Requirements Survey

- Sent out survey in spring 2013 to OLCF project teams
- Received responses from 21 code teams representing 18 projects across 15 science domains
- This was a large sample of the 31 INCITE projects representing 60% of resources allocated on OLCF systems.
- Science teams reaffirmed that they will not be able to meet their science goals at all or as fast without deployment of a system with significantly more capability than 30PF.

Hardware Feature Requirements

- Users were asked to rank the relative importance of hardware features for the next system
- In the past "more flops" has been the most important
- Now users are starting to feel the need for more memory bandwidth as well

Additional Parallelism in Applications

- Most users feel that they still have significant additional parallelism that can be extracted from their applications for future systems
- They are using a wide range of tools to access this parallelism, e.g., MPI, OpenMP, CUDA, OpenACC, libraries, OpenCL and Pthreads

Difficulty Exploiting Advanced Hardware

- Users are for the most part extraordinarily willing to exploit advanced hardware—to "do whatever it takes"
- However, they expressed concerns about lack of performance portability because of differing hardware and programming APIs and immaturity of some programming models

Assessment of difficulty in exploiting advanced hardware, by number of respondents

Adoption of Levels of Parallelism

• Most users surveyed indicated they had already adopted some form of node-level threading, either for CPU or accelerator

3. Application Readiness

- We went though an application readiness process for Titan (CAAR, Center for Accelerated Applications Readiness)
- We expect to have another readiness process for the OLCF-4 CORAL system
- We believe the lessons learned from the CAAR effort will help us

Center for Accelerated Application Readiness (CAAR)

WL-LSMS

Illuminating the role of material disorder, statistics, and fluctuations in nanoscale materials and systems.

S3D

Understanding turbulent combustion through direct numerical simulation with complex chemistry.

CAM-SE

LAMMPS

A molecular description of membrane fusion, one of the most common ways for molecules to enter or exit living cells.

mitigation scenarios; realistically represent features like precipitation patterns / statistics and tropical storms.

Answering questions about specific climate change adaptation and

NRDF

Radiation transport – important in astrophysics, laser fusion, combustion, atmospheric dynamics, and medical imaging – computed on AMR grids.

Denovo

Discrete ordinates radiation transport calculations that can be used in a variety of nuclear energy and technology applications.

> $\mathbb{R}^N \cap \mathbb{R}^N$ Slides courtesy Bronson Messe Vational Laborator

Application characteristics inventory

Code Changes for Titan

Some Lessons Learned

- Projects were successful obtaining substantial code performance improvements using the GPUs
- 70-80% of developer time was spent in code restructuring, regardless of the parallel API used. Because of this, we feel confident that the porting effort will make it much easier to port these codes to OLCF-4.
- Codes need as much lead time as possible to prepare for a substantially different computing system

Some Lessons Learned

- Some codes are more easy to port than others, depending on various factors:
	- Code execution profile—flat or hot spots
	- The code size (LOC)
	- Structure of the algorithms—e.g., available parallelism, high computational intensity
- Since this was a new effort and tools were not mature, the port required 1-3 person-years per code. We expect now for this to be much shorter.

Performance Portability

- The diversity of new kinds of system and programming API is making performance portability a growing concern (NVIDIA, Intel, AMD, …)
- The industry is consolidating into a fairly uniform configuration of hierarchical parallelism in the form of vector/multithreading/core/socket/node/system
- Because of this uniformity, the 70-80% of porting effort spent on code restructuring can be leveraged across these architectures
- However, the lack of consolidation of programming APIs for this hardware makes code porting and maintenance needlessly difficult

API Standardization: Past Experience

Repeated pattern of hardware/API disruption, consolidation, standardization

Programming for Portability

- How codes are dealing with portability at present:
	- $-$ Interface to accelerated library with multiplatform support (LSMS)
	- Thin code layer with platform-specific interface (LAMMPS, Denovo)
	- Directives that can be changed for different platforms (S3D)
	- – C++ generic programming for composing platform-specific operations (Trilinos)
- What we can do
	- Urge vendors to agree upon performance portable standards and make these well-supported in software
	- In the meantime attempt to design codes defensively to prepare for future changes, e.g., isolate data layout issues from business logic of code

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Supplementary slides

Performance results:

How Effective are GPUs on Scalable Applications? OLCF-3 Early Science Codes

Very early performance measurements on Titan

Coming changes

- New developments announced by vendors
	- Burst buffers different checkpoint strategies, out-of-core algorithms
	- – 3-D stacked memory – changes balance of flop rate / memory speed; different caching structure
	- Self-hosting accelerators changes how latency-optimized vs. bandwidth-optimized code is combined
- More speculative
	- Application-level resiliency
	- Application-level power usage adaptivity
	- Extreme core counts per chip, e.g., Adapteva 64,000 cores by 2018
	- Intel CPU + FPGA on-die (???)
	- –Altera FPGA programmable with OpenCL (???)

