Porting The Spectral Element Community Atmosphere Model (CAM-SE) To Hybrid GPU Platforms

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Titan Workshop
What is CAM-SE?

- Climate-scale atmospheric simulation for capability computing
- Comprised of (1) a dynamical core and (2) physics packages
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**Dynamical Core**

1. “Dynamics”: wind, energy, & mass
2. “Tracer” Transport: (H$_2$O, CO$_2$, O$_3$, …)
   Transport quantities not advanced by the dynamics

http://esse.engin.umich.edu/groups/admg/dcmip/jablonowski_cubed_sphere_vorticity.png
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**Physics Packages**

Resolve anything interesting not included in dynamical core (moist convection, radiation, chemistry, etc)
Gridding, Numerics, & Target Run

• Cubed-Sphere + Spectral Element
• Each cube panel divided into elements
Gridding, Numerics, & Target Run

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Used CUDA FORTRAN from PGI
OACC Directives: Better software engineering option moving forward
Target 14km Simulations

- 16 billion degrees of freedom
Target 14km Simulations

• 16 billion degrees of freedom
  – 6 cube panels
Target 14km Simulations

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  – 110 prognostic variables

\[ \rho, \rho u, \rho v, p \]

\[ H_2O, CO_2, O_3, CH_4, \ldots \]
Target 14km Simulations

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- Scaled to 14,400 XT5 nodes with 60% parallel efficiency
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- Scaled to 14,400 XT5 nodes with 60% parallel efficiency
- Must simulate 1-2 thousand times faster than real time
- With 10 second CAM-SE time step, need \( \leq 10 \text{ ms} \) per time step
  - 32-64 columns of elements per node, 5-10 thousand nodes
CAM-SE Profile (XT5, 14km, 14K Nodes)

- Original CAM-SE used 3 tracers (20% difficult to port)
- Mozart chemistry provides 106 tracers (7% difficult to port)
  - Centralizes port to tracers with mostly data-parallel routines

### 3-Tracer CAM-SE
- Dynamics: 73%
- Physics: 16%
- Tracers: 7%
- Other: 4%

### 106-Tracer CAM-SE
- Dynamics: 22%
- Physics: 6%
- Tracers: 71%
- Other: 1%
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Fairly Easy To Port
Communication Between Elements

Process 0  Process 1
Physically occupy the same location, Spectral Element requires them to be equal

Edges are averaged, and the average replaces both edges
Communication Between Elements

**Implementation**

Edge_pack: pack all element edges into process-wide buffer. Data sent over MPI are contiguous in buffer.

Bndry_exchange: Send & receive data at domain decomposition boundaries

Edge_unpack: Perform a weighted sum for data at all element edges.

Physically occupy the same location, Spectral Element requires them to be equal

Edges are averaged, and the average replaces both edges
Original Pack/Exchange/Unpack

- Edge_pack ensures data for MPI is contiguous in buffer
- MPI communication occurs in “cycles”
Original Pack/Exchange/Unpack

• **Edge_pack** ensures data for MPI is contiguous in buffer
• **MPI communication occurs in “cycles”**
• A cycle contains a contiguous data region for MPI
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  - For each “send cycle”
    - Send cycle over PCI-e (D2H)
    - MPI_Isend the cycle
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  - For each “receive cycle”
    - MPI_Wait for the data
    - Send cycle over PCI-e (H2D)
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  - For each “receive cycle”
    - MPI_Wait for the data
    - Send cycle over PCI-e (H2D)
  - Unpack all edges in a GPU Kernel
Optimizing Pack/Exchange/Unpack

• For a cycle, PCI-e D2H depends only on packing that cycle
  – Divide edge_pack into equal-sized cycles
    1. Find only the elements directly involved in each separate cycle
    2. Evenly divide remaining elements among the cycles
  – Associate each cycle with a unique CUDA stream
  – Launch each pack in its stream
  – After a cycle is packed, call async. PCI-e D2H in its Stream
• Edge_unpack at MPI boundaries requires all MPI to be finished
• However, internal unpacks can be done directly after packing
Porting Strategy: Pack/Exchange/Unpack

- For each cycle
  - Launch `edge_pack` kernel for the cycle in a unique stream
  - Call a `cudaEventRecord` for the stream’s packing event
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Porting Strategy: Pack/Exchange/Unpack

- Prepost each cycle’s MPI_irecv
- While an MPI message remains pending
  - If all cycles finished packing (cudaEventQuery for all cycles’ pack)
    - Launch edge_unpack kernel over elements not dealing with MPI
  - For each cycle
    - If cycle finished packing (cudaEventQuery for the cycle’s pack)
      - Call async. PCI-e D2H copy for the cycle’s MPI data
      - Call cudaEventRecord for a PCI-e D2H event
    - If cycle finished D2H PCI-e (cudaEventQuery for the cycle’s D2H)
      - Call MPI_Isend for the cycle’s MPI data
    - If MPI data has been received (MPI_Test for the cycle’s transfer)
      - Call PCI-e H2D copy for the cycle’s MPI data
- Call a device-wide barrier to ensure PCI-e H2D copies are done
- Unpack elements dealing with MPI
Resulting Concurrency
Resulting Concurrency

GPU Kernels
Resulting Concurrency

GPU Kernels
PCI-e D2H
Resulting Concurrency

GPU Kernels
- PCI-e D2H
- PCI-e H2D
Resulting Concurrency

GPU Kernels
- PCI-e D2H
- PCI-e H2D
- MPI
Resulting Concurrency

- GPU Kernels
- PCI-e D2H
- PCI-e H2D
- MPI
- Host Computation
Other Important Porting Considerations

- Memory coalescing in kernels
  - Know how threads are accessing GPU DRAM, rethread if necessary
- Use of shared memory
  - Load data from DRAM to shared memory (coalesced)
  - Reuse as often as possible before re-accessing DRAM
  - Watch out for banking conflicts
- Overlapping kernels, CPU, PCI-e, & MPI
  - Perform independent CPU code during GPU kernels, PCI-e, & MPI
  - Break up & stage computations to overlap PCI-e, MPI, & GPU kernels
- PCI-e copies: consolidate if small, break up & pipeline if large
- GPU’s user-managed cache made memory optimizations that are more difficult on a non-managed cache
Porting Challenges

• Data structures: derived types of derived types of derived types of derived types
  – Very difficult for directives
• Interaction with the community
  – Reproducibility: bit for bit same answer across any MPI decomp
  – Likely useful to validate GPU-based results before science
  – Double precision is currently a requirement
• Dynamical core is still rapidly evolving
  – About to be accepted as the default core
  – This means lots of testing and changes
• CUDA Fortran: Still evolving
  – Many layers for something to go wrong. Hard to pinpoint.
  – New versions of compiler, CUDA, GPU, driver usually mean new bugs
Speed-Up: Fermi GPU vs 1 Interlagos / Node

- Benchmarks performed on XK6 using end-to-end wall timers
- All PCI-e and MPI communication included
Why Was Vertical Remap So Fast?

• Originally used splines for reconstruction
  – Splines require a linear solve $\rightarrow$ vertical dependence within loops
  – Vertical index could not be threaded, only horizontal

• We replaced reconstruction with Piecewise Parabolic Method
  – Vertically independent $\rightarrow$ vertical index was threaded $\rightarrow$ 30x more threads

• Original remapping used a summation to reduce flops
  – Summations are vertically dependent and harder to thread

• We changed it to do two integrations instead
  – This double the work for remapping
  – But it also reduced data requirements and dependence

• As a result, all data in the reconstruction and remap fit into cache
  – Only accesses to DRAM were at the very beginning and end of kernel with a lot of work in between, all done in-cache
  – Thus, >5x speed-up over PPM remap on CPU
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If Increasing The Workload
- Allows More Threading
- Decreases Data Dependence
- Decreases Local Data Requirements
- Then It’s Worth Investigating
Questions?
Usefulness Of Porting To Accelerators

- You understand your code’s challenges for many threads
- You will often refactor the algorithms themselves
  - Vertical remap: splines + summation $\rightarrow$ PPM + two integrations
  - More flops, but more independence and less data movement
- You will change the way you thread
  - Higher-level hoisting of OpenMP to allow more parallelism
  - More data-independent work, more flops
  - Better staging through cache, less data in cache (less thrashing)
- Incorporating changes into CPU code almost always speeds up the CPU code
  - This changes perspective on code refactoring cost-benefit
Think Differently About Threading

**CPU Code**

```c
do ie=1,nelemd
  do q=1,qsize
    do k=1,nlev
      do j=1,np
        do i=1,np
          coefs(1,i,j,k,q,ie) = ...
          coefs(2,i,j,k,q,ie) = ...
          coefs(3,i,j,k,q,ie) = ...
        enddo
      enddo
    enddo
  enddo
enddo
```

**GPU Code**

```c
ie = blockIdx%y
q  = blockIdx%x
k  = threadIdx%z
j  = threadIdx%y
i  = threadIdx%x
coefs(1,i,j,k,q,ie) = ...
coefs(2,i,j,k,q,ie) = ...
coefs(3,i,j,k,q,ie) = ...
```
Think Differently About Threading

CPU Code

\[
\text{do } ie=1,\text{nelemd} \\
\text{do } q=1,\text{qsize} \\
\quad \text{do } k=1,\text{nlev} \\
\quad \quad \text{do } j=1,\text{np} \\
\quad \quad \quad \text{do } i=1,\text{np} \\
\quad \quad \quad \text{coefs}(1,i,j,k,q,ie) = \ldots \\
\quad \quad \quad \text{coefs}(2,i,j,k,q,ie) = \ldots \\
\quad \quad \quad \text{coefs}(3,i,j,k,q,ie) = \ldots \\
\]

Coded to respect cache locality

GPU Code

\[
\text{ie} = \text{blockidx}\%y \\
\text{q} = \text{blockidx}\%x \\
\text{k} = \text{threadidx}\%z \\
\text{j} = \text{threadidx}\%y \\
\text{i} = \text{threadidx}\%x \\
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do k=1,nlev 
do j=1,np 
do i=1,np 
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Coded to respect cache locality

However, these will not be sequential accesses on GPUs
Think Differently About Threading

**CPU Code**

```
do ie=1,nelemd
  do q=1,qsize
    do k=1,nlev
      do j=1,np
        do i=1,np
          coefs(1,i,j,k,q,ie) = ...
          coefs(2,i,j,k,q,ie) = ...
          coefs(3,i,j,k,q,ie) = ...
        end do
      end do
    end do
  end do
end do
```

**Memory accessed in the order of instructions**
- `coefs(1,1,1,1,...)`
- `coefs(2,1,1,1,...)`
- `coefs(3,1,1,1,...)`
- `coefs(1,2,1,1,...)`
- `coefs(2,2,1,1,...)`
- ...

**GPU Code**

```
ie = blockIdx%y
q  = blockIdx%x
k  = threadIdx%z
j  = threadIdx%y
i  = threadIdx%x
coefs(1,i,j,k,q,ie) = ...
coefs(2,i,j,k,q,ie) = ...
coefs(3,i,j,k,q,ie) = ...
```

**Memory accessed in the order of threads**
- `coefs(1,1,1,1,...)`
- `coefs(1,2,1,1,...)`
- `coefs(1,2,1,1,...)`
- `coefs(1,N,1,1,...)`
- `coefs(1,1,2,1,...)`
- `coefs(1,2,2,1,...)`
Think Differently About Threading

**CPU Code**

```plaintext
do ie=1,nelem
do q=1,qsize
do k=1,nlev
do j=1,np
do i=1,np
coeffs(1,i,j,k,q,ie) = ...
coeffs(2,i,j,k,q,ie) = ...
coeffs(3,i,j,k,q,ie) = ...
```

**GPU Code**

```plaintext
ie = blockIdx%y
def = blockIdx%x
k = threadIdx%z
j = threadIdx%y
i = threadIdx%x
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coeffs(2,i,j,k,q,ie) = ...
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            coefs(2,i,j,k,q,ie) = ... 
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   end do 
end do 
end do 
end do 
```

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j  = threadIdx%y
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coefs(i,j,k,q,ie,1) = ... 
coefs(i,j,k,q,ie,2) = ... 
coefs(i,j,k,q,ie,3) = ...
```

- Memory accessed in the order of **threads**
  - coefs(1,1,1,...)
  - coefs(2,1,1,...)
  - ...
  - coefs(N,1,1,...)
  - coefs(1,2,1,...)
  - coefs(2,2,1,...)